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The Impact of Layout Dependent Parasitic RLC on High Frequency Performance in 3T and 4T MF nMOSFETs

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Abstract

A new observation of significant differences in the high frequency device parameters and performance like f_T and f_{MAX} is identified from the comparison of 3-terminal (3T) and 4-terminal (4T) multi-finger (MF) nMOSFETs. Through an extensive characterization on the intrinsic Z- and Y-parameters, it is found that the major impact comes from the particular increase of intrinsic parasitic RL at the source terminal, namely $R_{s,int}$ and $L_{s,int}$ in the 4T MF MOSFETs. The proposed analytical models as a function of key device parameters incorporating the influence of the intrinsic parasitic RLC through high frequencies can accurately predict f_T and f_{MAX} degradation in 4T MF nMOSFETs as well as the complicated layout dependent effects. The experimental results and analytical models can be useful to facilitate MF devices layout optimization for high frequency design and performance improvement.

I. Introduction

MF MOSFETs have been widely used in high frequency (RF/mm-wave) and analog circuits for gate resistance (R_g) reduction, which is considered the key factor for achieving higher f_{MAX} and lower noise in terms of R_n and NF_{min} [1]. However, very narrow finger width (W_F) associated with very large finger number (N_F) may lead to the penalties, such as the increase of finger-end fringing capacitances ($C_{f(poly\text{-}end)}$) and parasitic source resistances (R_S), which may bring adverse impact on f_T and f_{MAX} [2]-[3]. Moreover, how to determine the real R_g responsible for f_{MAX} becomes a fundamental topic with open questions to the conventional methods [4]-[5]. Regarding the configuration for biasing, 3-terminal (3T) MOSFETs with source and body (S/B) internally tied together has been a standard offering adapted to 2-port characterization and modeling, but limited to common source (CS) topology. Thus, 4-terminal (4T) MF MOSFETs with separate source and body appears as an important feature to realize various circuit topologies like CS, common gate (CG), and common drain (CD), given with freedom in body biases for low voltage and low power design [6]. However, the potential differences between the 3T and 4T MF MOSFETs in high frequency characteristics and performance, as well as equivalent circuit model even under CS condition, emerge as a critical issue not well understood. The mentioned topics motivate our research effort in this paper.

II. 3T and 4T MF devices layouts and Characterization

MF nMOSFETs and openM1 deembedding structures were fabricated in 90nm CMOS process with the layouts, illustrated in Fig. 1(a)~(d), such as W2N16, W05N64, and W025N128, at fixed $W_{tot}=W_F\times N_F=32$ μm. Note that the gate length is pushed to $L_g=55$nm for achieving peak f_T above 170GHz. Fig. 2(a) and (b) present the layouts of 3T and 4T MF MOSFETs with source and body internally shorted and separated, respectively. The 3T MOSFETs can fit 2-port test structure with $V_S=V_B$ to common ground but are limited to CS topology at zero body bias ($V_{BS}=0$). On the other hand, 4T MOSFETs can enable various circuit topologies like CS, CG, and CD, as well as variable V_{BS}. In this paper, 3T and 4T MOSFETs with the same MF layouts (Fig.1) were allocated in 2-port test structure with the S/B connected to ground pad for a comprehensive characterization and comparison to investigate any differences or impact on the high frequency characteristics and performance. Note that the 4T MOSFETs with internal S/B separated but external S/B shorted to the ground pad may introduce uncertainty at the internal V_{BS} and influence on the intrinsic parasitic RL due to separate interconnect to the internal S/B.

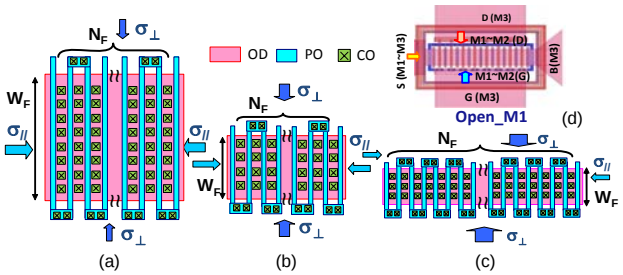

Fig. 1 Layout of MF MOSFETs with $W_F\times N_F$ =32μm (a) W2N16 (b) W05N64 (c) W025N128 (d) openM1 deembedding structure.

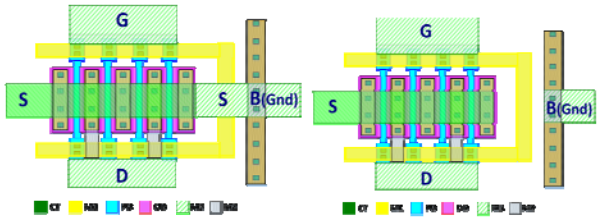

Fig.2 Multi-finger MOSFET layouts (a) 3-terminals (3T) with source and body internally tied together (b) 4-terminals (4T) with source and body internally separated.

III. High Frequency Performance and Intrinsic Parasitic RL – 3T and 4T MF nMOSFETs

Fig. 3(a) presents f_T determined by the unit current gain, i.e. $f_T=f(|H_{21}|=1)$. The results indicate drastic degradation of f_T corresponding to the smaller W_F and larger N_F for both 3T and 4T MF nMOS. The peak f_T can reach 172GHz for W2N16_3T but suffers more than 27% drop to only 125GHz for W025N128_3T. The increase of gate capacitance C_{gg} due to $C_{f(poly\text{-}end)}\times N_F$ is considered as one major root cause [1]-[2]. What even worse, the 4T MF nMOS reveal the drawback of lower f_T compared to the 3T counterparts, and the larger N_F leads to worse degradation up to 10% in case of W025N128. As shown in Fig. 3(b), the f_{MAX} defined by unit power gain, i.e. $f_{MAX}=f(|U|=1)$ indicates apparently lower f_{MAX} in 4T nMOS than 3T counterparts for all three MF layouts. The peak f_{MAX} can be as high as 225 GHz for W05N64_3T but suffers around 17% drop to 187 GHz for W05N64_4T and even worse to 178 GHz for W025N128_4T. Note that the f_{MAX} degradation suffered by 4T nMOSFETs dominates the difference between various MF layouts. Through an equivalent circuit analysis on the MF nMOSFETs under cold device condition ($V_{DS}=0$, $V_{GS}>V_T$) shown in Fig. 4(a), the intrinsic parasitic resistances at source and drain, i.e. $R_{s,int}$ and $R_{d,int}$ can be extracted from the $Re(Z_{12})$ and $Re(Z_{22})$ at lower frequencies. The results shown in Fig. 5(a) indicate much larger $R_{s,int}$ from 4T MF nMOS in case of larger N_F but similar $R_{d,int}$ in 3T and 4T MF nMOS. Furthermore, through equivalent circuit analysis under saturation condition ($V_{DS}=V_{DS}$, $V_{GS}>V_T$) shown in Fig. 4 (b), the intrinsic parasitic inductances at source and drain, i.e. $L_{s,int}$ and $L_{d,int}$ can be extracted by the best fitting to 2-port Y-parameters including $Re(Y_{21})$. The results shown in Fig. 5(b) indicate much larger $L_{s,int}$ in 4T MF nMOS, which will result in significant degradation of $Re(Y_{21})$ at higher frequency and then

further impact on f_T and f_{MAX}. The peak f_{MAX} can be as high as 225 GHz for W05N64_3T but suffers around 17% drop to 187 GHz for W05N64_4T and even worse to 178 GHz for W025N128_4T. Note that the f_{MAX} degradation suffered by 4T nMOSFETs dominates the difference between various MF layouts.

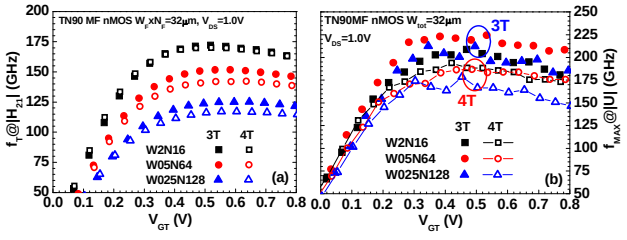

Fig. 3 Comparison of 3T and 4T nMOSFETs with 3 sets of MF layouts W2N16, W05N64, W025N128 (a) f_T@$|H_{21}|$=1 (b) f_{MAX}@$|U|$=1 at V_{DS}=1.0V and various V_{GT}

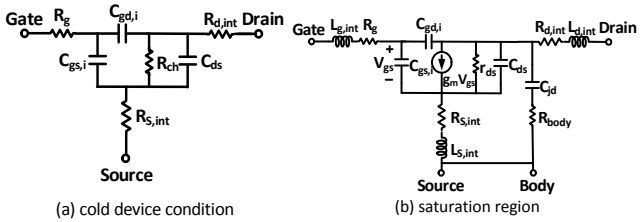

Fig. 4 Equivalent circuit models for MF MOSFET (a) cold device condition V_{DS}=0, $V_{GS} > V_T$ (b) saturation condition at V_{DS}= V_{DD}, $V_{GS} > V_T$

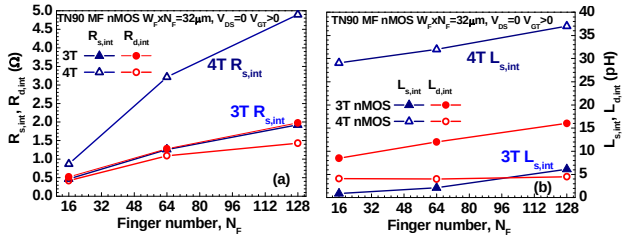

Fig. 5 The intrinsic parasitic RL extracted from 3T and 4T MF nMOSFETs with layouts W2N16, W05N64, W025N128 (a) $R_{s,int}$ and R_{dint} vs. N_F (b) $L_{s,int}$ and L_{dint} vs. N_F after deembedding, at V_{DS}=0 and V_{GS}=1.0V

The detrimental impact from the significant increase of $R_{s,int}$ and $L_{s,int}$ on f_T and f_{MAX} in 4T MF nMOS has been verified as follows. First, Fig. 6 (a)~(c) present key device parameters, such as g_m@Y=Re(Y_{21}), C_{gg}=Im(Y_{11})/ω, and C_{gd}= -Im(Y_{12})/ω at high frequencies, and the f_T calculated by the analytical model (1), shown in Fig. 6(d). Unfortunately, the 4T MF nMOS reveal 17.6%~28.6% degradation of g_m compared to the 3T counterparts, as shown in Fig. 6 (a), which is caused by the dramatic increase of $R_{s,int}$ and $L_{s,int}$ in 4T MF nMOS **(**Fig. 5). Interestingly, the C_{gg} shown in Fig.6(b) indicates similar trend, such as 9.87%~15.6% less C_{gg} in 4T MF nMOS than the 3T counterparts, due to the same reason, i.e. $R_{s,int}$ and $L_{s,int}$. It means that the C_{gg} reduction can make partial compensation to the g_m degradation but cannot recover the loss of f_T according to (1) due to 6~14% more reduction in g_m than C_{gg}. The f_T@model calculated by (1) (Fig. 6(d)) show a good match with the f_T@($|H_{21}|$=1) in which the f_T degradation can be up to 10% for W025N128_4T compared to W025N128_3T. Note that The peak f_T can reach above 170GHz for W2N16 but suffers 27~31% drop to only 125~117 GHz for W025N128. The increase of C_{gg} due to $C_{f(poly\text{-}end)}$×N_F in case of larger N_F shown in Fig.6(b) was identified as the root cause for f_T degradation [1]-[2]. Further investigation has been performed on the f_{MAX} shown in Fig. 7 in which the 4T MF nMOS indicate f_{MAX} degradation of 6.8% for W2N16 and much worse to 17.7% in case of W025N128. This dramatic degradation can be understood from the analytical model for f_{MAX} given by (2) revealing the major impact from R_g@Y and $R_{s,int}$. The lower f_T will lead to lower f_{MAX} but the drastic increase of $R_{s,int}$ in 4T MF nMOS shown in Fig. 7(c) appears as the major factor responsible for obviously worse degradation of f_{MAX} than f_T. As for R_g@Y shown in Fig.7(d), that is another key parameter responsible for f_{MAX} degradation, there is minor difference between 3T and 4T MF nMOS in case of W2N16 and W05N64 but apparently larger R_g@Y in W025N128_4T than W025N128_3T, due to the significant increase of $L_{s,int}$.

$$f_T = \frac{g_m@Y}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}},\ g_m@Y = \mathrm{Re}(Y_{21}), C_{gg} = \frac{\mathrm{Im}(Y_{11})}{\omega}, C_{gd} = \frac{-\mathrm{Im}(Y_{12})}{\omega} \quad (1)$$

$$f_{MAX} = \frac{f_T}{2\sqrt{R_g@Y(g_{ds} + 2\pi f_T C_{gd}) + g_{ds}R_{s,int}}},\ R_g@Y = \frac{\mathrm{Re}(Y_{11})}{\left[\mathrm{Im}(Y_{11})\right]^2} \quad (2)$$

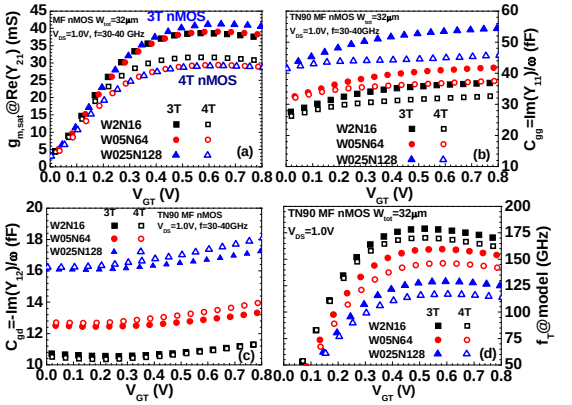

Fig.6 Comparison of 3T and 4T MF nMOSFETs with various layouts W2N16, W05N64, W025N128 (a) g_m=Re(Y_{21}) (b)C_{gg}= Im(Y_{11})/ω(c)C_{gd}=-Im(Y_{12})/ω (d) f_T model=$g_m/2\pi(C_{gg}^2 - C_{gd}^2)^{1/2}$, V_{DS}=1V and various V_{GT}

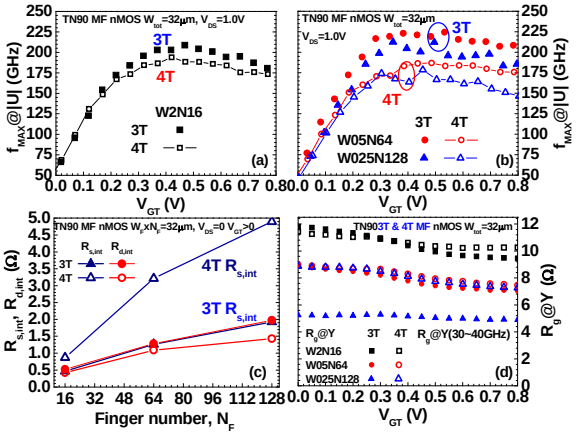

Fig. 7 Comparison of 3T and 4T MF nMOSFETs (a) f_{MAX}@$|U|$=1 for W2N16 (b) f_{MAX}@$|U|$=1 for W05N64 and W025N128 at V_{DS}=1.0V and various V_{GT} (c) $R_{s,int}$ and R_{dint} (d) R_g@Y=Re(Y_{11})/[Im(Y_{11})]^2 (30~40GHz)..

IV. Conclusion

4T MF MOSFETs have been the choice to enable various circuit topologies like CS, CG, and CD, as well as dynamic body biases for low voltage and low power design. However, the 4T MF nMOSFETs reveal dramatic degradation of f_T and f_{MAX} up to 10% and 17.7% in case of W025N128. The significant increase of $R_{s,int}$ and $L_{s,int}$. is identified as the root cause responsible for the g_m degradation and increase of R_g@Y, and thus further impact on f_T and f_{MAX}. The proposed analytical models can accurately predict f_T and f_{MAX} with layout dependent effects in 3T and 4T MF nMOSFETs. For CS topology with zero body bias, 3T MF MOSFETs should be the choice for higher f_T and f_{MAX}. As for the other circuit topologies, 4T MF MOSFETs employing some innovative layout solutions for effective reduction of the intrinsic parasitic RLC deserves more extensive research effort.

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