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Defect Decoupling for Polycrystalline Silicon MOSFETs using a Single Pulse Charge Pumping Method

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Abstract

"An application of single pulse charge pumping method was proposed to decouple interface trap and grain boundary trap density in floating body (FB) poly-crystalline silicon (poly-Si) metal-oxide-semiconductor field-effect-transistor (MOSFET). The linear dependence of the total trap density on the poly-Si thickness was used to extract the interface trap density at the extrapolation point. The method presents advantages of fast measurement, simplicity in theory, and high resolution of defect density."

1. Introduction

Poly-Si MOSFETs have been introduced in various applications such as driving in display, 3D memory, and 3D CMOS integrated circuits [1-3]. In poly-Si, grain boundary (GB) contains a number of defects which strongly affect to the device performance and reliability. The defects with fast response time (shallow traps) would reduce carrier mobility in high frequency applications while the deep traps affect to the erase time in memory applications. GB defect characterization and passivation is a must in advance applications of poly-Si MOSFETs.

In this study, a single pulse charge pumping method is applied to measure the total defect density (N_{POLY}) in the FB poly-Si MOSFETs. A simple physical model of the poly-Si MOSFET was used to decouple the interface defect density (N_{IT}) and GB defect density (N_{GB}). In combination with a quasi-static capacitance-voltage (QSCV) measurement, the defect profiles of GB and interface defect density in the energy band-gap was successfully extracted for the poly-Si MOSFETs with various channel thicknesses.

2. Defect decoupling

Defect decoupling principle is illustrated in Fig. 1. Poly-Si MOSFETs were fabricated with same grain size and different thicknesses ($t_{poly\text{-}Si}$ of 7 nm, 10 nm, 13 nm, and 16 nm) so that N_{POLY} would be linear with t_{POLY}. Therefore, the extrapolation of N_{POLY} versus t_{POLY} plot is determined as N_{IT}. As a result, the grain boundary trap density can be extracted using $N_{GB} = N_{POLY} - N_{IT}$. To have same grain size with different thicknesses of poly-Si, these poly-Si layers were etched from a 23-nm-thick undoped poly-Si to reach the corresponding thicknesses. An n-doped junction was made by ion implantation and thermal activation to form low-resistance-contact with the poly-Si channel.

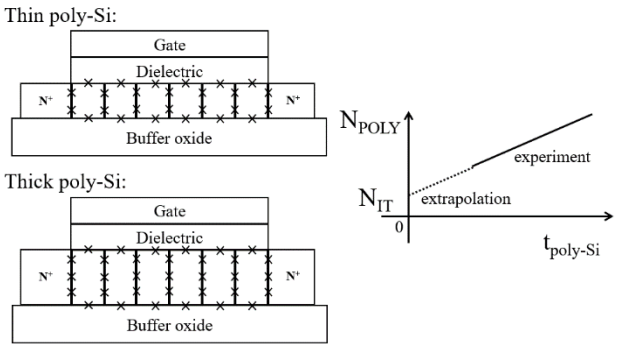

Fig. 1 Principle to decouple the interface defect density from the total defect density.

An SPCP was applied on a poly-Si MOSFETs to characterize N_{POLY} [4]. The SPCP set-up was illustrated in Fig. 2a. A pulse was applied on the gate with the ramping rate of 10^5 V/s while the carrier transport current (I_{SPCP}) was measured at the n-doped junction. The base voltage of gate pulse was set below flat band voltage of -0.5 V. The amplitude of the gate pulse is increased to detect N_{POLY} at various position in the band-gap. During the rise time, electrons accumulate into the channel and contribute to free electrons and trapped electrons. During the fall time, the free electrons escape out of the poly-Si channel and leave the trapped electrons. Therefore, the net charge recorded at the end of the fall edge of the gate pulse was converted into charge density using following equation:

$$N_{POLY} = \int_{o}^{t} \frac{I_{SPCP}}{q * Area} dt \qquad (1)$$

The distribution of traps at the interface, D_{IT} ($cm^{-2}eV^{-1}$), and the normalized distribution of grain boundary traps in the poly-Si channel, D_{GB} ($cm^{-3}eV^{-1}$), was calculated using N_{IT}, N_{GB} and effective band bending (ψ) in poly-Si channel:

$$\psi = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_{QSCV}}{C_{OX}}\right) dV_G \,, \qquad (2)$$

$$D_{IT} = \frac{\partial N_{IT}}{\partial \psi}, \quad (3)$$

and $$D_{GB} = \frac{1}{t_{poly-Si}} \frac{\partial N_{GB}}{\partial \psi}. \quad (4)$$

Figure 2b shows the total trap density of the poly-Si samples measured by the SPCP method. The gate pulse amplitude was varied (with a constant ramp rate) to detect N_{POLY} with different band bending in the poly-Si channel. N_{POLY} increases with the increase of poly-Si thickness, which is resulted from thickness dependence of N_{POLY} because of the defects at the GB. In other words, the increase of N_{POLY} with $t_{poly-Si}$ could be explained by the contribution of N_{GB} into N_{POLY}. N_{POLY} increases significantly with V_G around the depletion region (from -1 V to 1 V), which is due to the deep trap states. We should notice that the n-type junction limits the transportation of holes going through the junction. In other words, using n-type doped junction only allows to characterize the electron traps.

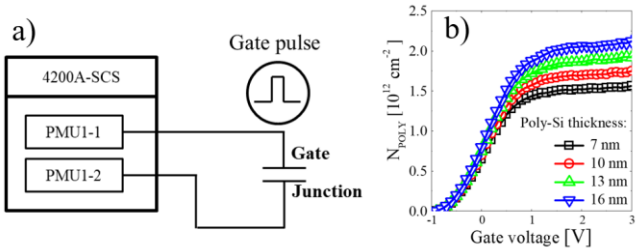

Fig. 2 Defect measurement using the SPCP: measurement setup (a) and total defect density (b).

To decouple N_{IT} and N_{GB} from N_{POLY}, N_{IT} was extracted from the intercept of N_{POLY} versus $t_{poly-Si}$ plots (see Fig. 3a). Therefore, N_{GB} was calculated as $N_{POLY} - N_{IT}$. N_{IT} and N_{GB} were summarized in Fig. 3b. The interface trap density dominates in the total traps in the poly-Si devices used in this study. However, the grain boundary traps also take a significant proportion in the total traps, which is linear with the poly-Si channel thickness. The sample with thinner poly-Si thickness contains less contribution of N_{GB} in the total trap density, which is one of the important benefits to reduce the poly-Si channel thickness.

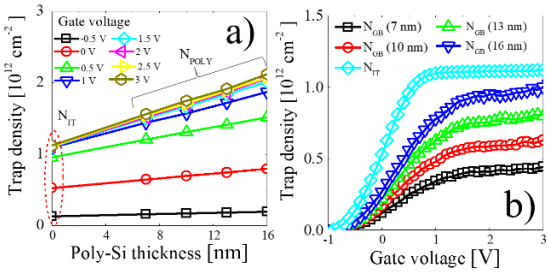

Fig. 3 Defect decoupling: N_{IT} extraction (a) and field dependent defect density in the poly-Si MOSFETs with various $t_{poly-Si}$ (b).

The distribution of the interface traps and the normalized distribution of grain boundary traps were shown in Fig. 4. The distribution of grain boundary traps (normalized by the channel thickness) is similar for all samples (see Fig. 4a), which implies that the defect decoupling is successful. A number of dangling bonds were detected near the mid-gap region (peak at 0.38 eV below the conduction edge). The interface trap density (see Fig. 4b) also contains a significant number of deep traps, which must be the existence of the dangling bonds near the interface. Minimum detectivity of this method is about $3*10^{17}$ $cm^{-3}eV^{-1}$ for D_{GB} and $6*10^{12}$ $cm^{-2}eV^{-1}$ for D_{IT} extraction.

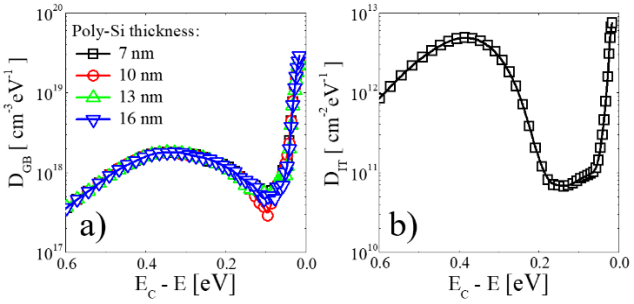

Fig. 4 Defect distribution of defects in the silicon band gap located at the grain boundaries (a) and the interface (b).

3. Conclusions

We demonstrated a defect decoupling method for the poly-Si MOS devices using the linear dependence of the total traps on the channel thickness. The distribution of deep trap states was extracted successfully with good detectivity. The results open more opportunity of using the SPCP method for disordered semiconductor based MOS devices.

References

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