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Study on Random Telegraph Noise of High-κ/Metal-Gate Gate-All-Around Poly-Si Nanowire Transistors

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Abstract

We report random-telegraph-noise (RTN) characteristics of gate-all-around (GAA) poly-Si nanowire (NW) transistors with high-k oxide/metal-gate (HK/MG) stack. Clear two-level RTN signals are detected from devices with effective channel length of 150 nm and width of 30 nm. Through extensive analysis, we identified the trap spatially locating within the interfacial layer (IL) and away from the IL/channel interface with a distance of 0.4nm.

1. Introduction

Multiple-gate [1] in combination with HK/MG [2] device schemes are great technology enablers to improve the gate controllability and to suppress short-channel effects for ultra-short-channel transistors. In line with the aggressive device downscaling, the impact of RTN becomes more significant [3]-[4]. However, there are few reported studies on RTN of transistors with GAA and HK/MG. In this work, we report the experimental RTN measurements and analysis on HK/MG GAA poly-Si junctionless (JL) NW transistors.

2. Devices Fabrication

Figure 1(a) illustrates the schematic structure of the studied HK/MG GAA poly-Si JL NW transistors. The fabrication process flow is almost the same with the one reported in our previous work [5] except that the gate stack is replaced by HK/MG. In brief, following the poly-Si NWs were suspended, the samples were immersed into a H_2O_2 solution for 5 minutes at 100ºC to grow a chemical SiO_2 as the interfacial layer (IL). Then, a 5nm-thick HfO_2 layer was deposited as gate oxide by using an atomic layer deposition (ALD) system, followed by a post deposition annealing at 500 ºC for 30 s. A 5nm-thick ALD TiN layer and a 150nm-thick sputtered TiN layer were sequentially deposited and lithographically patterned as the metal gate. Finally, standard metallization processes completed the HK/MG GAA poly-Si JL NW transistors fabrication.

3. Results and Discussion

Figure 1(b) displays the transmission electron microscopic (TEM) micrograph of a fabricated poly-Si JL NW transistor along the YY' cut-line direction as indicated in Fig. 1(a). The thicknesses of HK oxide (T_{HK}) and interfacial layer (T_{IL}), as well as the channel radius (R) are identified to be 4.7, 1.2, and 4.3 nm, respectively. Subthreshold swing (SS) and threshold voltage (V_{TH}) extracted from the I_D-V_G characteristics shown in Fig. 2 for transistors with L_{eff} = 150 nm are 104 mV/decade and 0.73 V, respectively. Figure 3 shows clear time-domain RTN signals measured at various V_G. It is clearly seen in Fig. 4(a) that there are two-level current peaks in the histogram plots cumulating all the measured drain current values. Similarly, we have also observed typical two-level current peaks from the corresponding time-lag plots [6] using kernel density estimation scheme [7] as shown in Fig. 4(b).

We are able to estimate the spatial location of the trap contributing RTN by using the formula summarized in Table 1 based on a theory proposed by a previous report [8]. We assumed the location of the trap (radial distance from the channel surface) being either within the IL ($X_{T,IL}$) or within the HK ($X_{T,HK}$) layers, and the corresponding spatial locations are derived in Eqs. (1) and (2), respectively in Table I. From Fig. 3, extracted capture and emission time constants of τ_c and τ_e, respectively, are 3.6ms ~ 0.4ms and ~0.5ms at V_G ranging from 1.1V–1.3V (Fig. 5(a)). Thus, we can get the logarithmic ratio of τ_c and τ_e with respect to V_G depicted in Fig. 5(b) in which the slope of the fitting curve is -10.35. The value is then used to extract $X_{T,IL}$ (Eq. (1)) and $X_{T,HK}$ (Eq. (2)) which are found to be 0.4nm (Fig. 6) and -3.3 nm, respectively. Obviously, the trap is located in IL as the negative value for $X_{T,HK}$ is unreasonable.

3. Conclusions

We have successful fabricated short-channel (L_G = 150nm) GAA poly-Si NW transistors with HK/MG. Because of the short effective channel length (150 nm) and width (3 nm), clear two-level RTN characteristics have been observed. From the analysis of trapping depth extraction, the trap is supposed to be located within the IL with the spatial depth of approximately 0.4 nm from the IL/channel interface.

Acknowledgements

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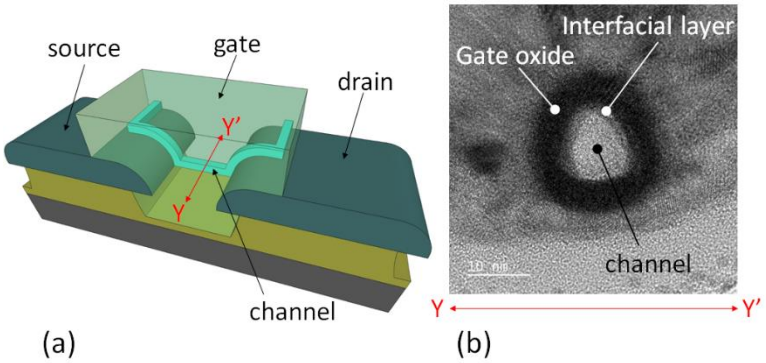

Fig. 1 (a) Schematic structure and (b) TEM image of a test device.

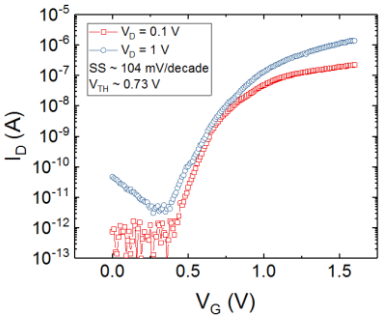

Fig. 2 Transfer characteristics of a fabricated poly-Si NW JL FETs with L_G = 150nm.

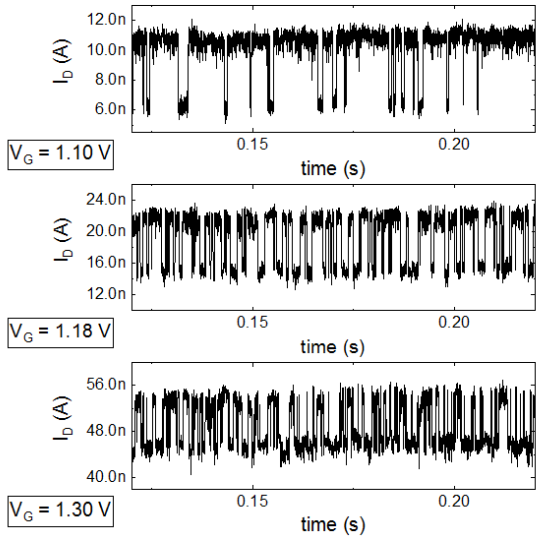

Fig. 3 Time-domain I_D RTN signals at varies V_G.

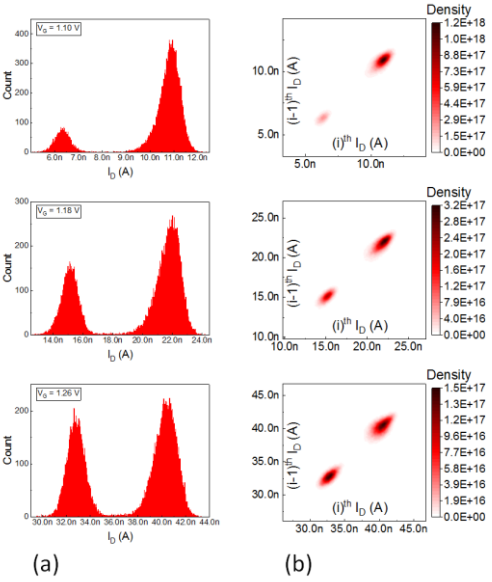

Fig. 4 (a) I_D histogram plots. (b) Time-lag density plots.

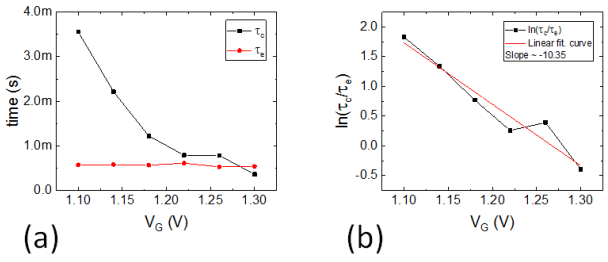

Fig. 5 (a) The time constant and (b) $\ln(\tau_c/\tau_e)$ at varies V_G.

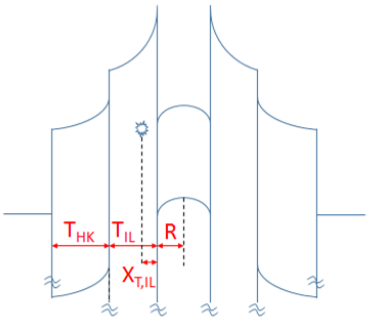

Fig. 6 The band diagram of trap in IL model.

Table I X_T extraction formula while trap in IL and HK.

For trap in IL:	$X_{T,IL} \cong \left\{\left(1+\frac{T_{IL}}{R}\right)^{\left[\left(-\frac{KT}{q}\right)(1+\xi)\left(\frac{d}{dV_G}\ln\left(\frac{\tau_c}{\tau_e}\right)\right)\right]}-1\right\}R$	(1)
For trap in HK:	$X_{T,HK} \cong \left\{\left(1+\frac{T_{ox}}{R+T_{IL}}\right)^{\left[\left(-\frac{KT}{q}\right)(1+1/\xi)\left(\frac{d}{dV_G}\ln\left(\frac{\tau_c}{\tau_e}\right)\right)-1/\xi\right]}-1\right\}(R+T_{IL})$	(2)
	$\xi = \frac{\varepsilon_{IL}}{\varepsilon_{ox}}\log_{\left(\frac{R+T_{IL}}{R}\right)}\left(1+\frac{T_{ox}}{R+T_{IL}}\right)$	(3)