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Systematic analysis of electron traps of HfSiON/SiO_2 nMOSFETs using TSCIS

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Abstract

This paper proposes a quantitative oxide trap profiling method for both pre-existing and stress-induced oxide traps using trap spectroscopy by charge injection and sensing (TSCIS) and investigates positive bias temperature instability (PBTI) mechanism of HfSiON/SiO_2 nMOSFETs based on the extracted oxide traps. The extracted pre-existing traps and PBTI-induced traps are located at ~0.3 eV and ~0.8 eV below the HfSiON conduction band edge. The experimental results indicate that the energy level of electron traps can be shifted downward due to lattice relaxation once electrons are trapped at pre-existing traps by PBTI stress.

1. Introduction

The oxygen vacancies in high-k dielectric act trap/de-trap sites of electrons or holes and can be generated additionally by BTI [1-4]. K. Torii et al. reported that the empty oxygen vacancies (V_o^{2+}) in high-k dielectric act electron trapping sites and oxygen vacancies level is shifted downward for V_o^+ and V_o due to lattice relaxation [5].

The distribution of oxide defects be investigated by trap spectroscopy by charge injection and sensing (TSCIS) method [6]. TSCIS method is consistent and quantitative model for pre-existing oxide trap. However, high-k nMOSFETs have large polarizability [7] and oxygen vacancies in high-k dielectric can be shifted downward due to PBTI, so both pre-existing and PBTI-induced oxygen vacancies have to be investigated for identifying PBTI mechanism and reliability of high-k nMOSFETs.

This paper proposes a quantitative oxide trap profiling method for both pre-existing and PBTI-induced oxygen vacancies and investigates PBTI mechanism of HfSiON/SiO_2 nMOSFETs based on the extracted oxygen vacancies in HfSiON.

2. Experimental devices

The devices for the experiment were nMOSFET with gate length L = 48 nm and gate width W = 10 μm, which are fabricated using 48 nm CMOS technology. The n^+ poly-Si gate electrode was formed on the TiN layer which was deposited on top of HfSiON by atomic layer deposition. The gate dielectric material consisted of a 3-nm-thick HfSiON layer and a 1-nm-thick SiO_2 interfacial layer. All electrical parameters were measured using an Keysight B1500A semiconductor device analyzer. The parameters for oxide trap profiling are listed in Table 1.

Table 1 The parameters for oxide trap profiling

Parameter	Notation	Value
ϕ_1	Si/SiO_2 barrier heights	3.2 eV
ϕ_2	$HfSiON/SiO_2$ barrier heights	1.7eV
t_{IL}	SiO_2 thickness	1 nm
t_{hk}	HfSiON thickness	3 nm
ε_s	Si dielectric constant	11.7
ε_{IL}	SiO_2 dielectric constant	3.9
ε_{hk}	HfSiON dielectric constant	15
m_{IL}	Relative electron mass in SiO_2	$0.5m_o$
m_{hk}	Relative electron mass in HfSiON	$0.24m_o$
σ_{IL}	Electron capture cross section in SiO_2	1×10^{-18} cm^2
σ_{hk}	Electron capture cross section in HfSiON	1×10^{-18} cm^2

3. Results and Discussion

The trap level of oxygen vacancies in high-k dielectric can be changed when PBTI stress is applied to gate, so both pre-existing and PBTI-induced oxygen vacancies have to be investigated for identifying PBTI mechanism accurately. The proposed algorithm to extract both pre-existing and PBTI-induced traps was represented by following flow chart (Fig. 1).

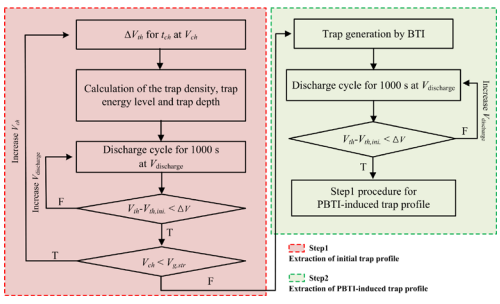

Fig. 1 The algorithm of oxide trap profiling

For applying the algorithm, it is necessary to divide charge voltage (V_{ch}) and stress voltage ($V_{g,str}$). The separation of V_{ch}

and $V_{g,str}$ was determined by the stress-induced leakage current (SILC), which is calculated from pre-stress gate current I_g(fresh) and post-stress gate current I_g(stressed). The SILC at V_g=1.0 V was measured at different $V_{g,str}$ (Fig. 2).

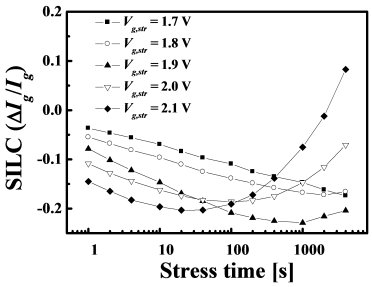

Fig. 2 The SILC for separation of V_{ch} and $V_{g,str}$.

The decrease of SILC means electron trapping at pre-existing traps in HfSiON and the increase of SILC means newly trap generation [8]. The results of SILC in HfSiON/SiO_2 nMOSFET showed that both initial trapping and newly trap generation was increased with increasing $V_{g,str}$ and newly traps were generated at early stress time when $V_{g,str}$ was increased. However, SILC at $V_{g,str}$ = 1.7 V was decreased consistently with increasing t_s, it means that electron trapping occurs only in range of $V_{g,str} \leq 1.7$ V. Thus, V_{ch} was determined in range of $V_g \leq 1.7$ V.

The algorithm in Fig. 1 had two-step procedure for initial trap and PBTI-induced trap respectively. At charge cycle for initial trap profile of step1, V_{th}-shift (ΔV_{th}) was measured with increasing charge time (t_{ch}) at V_{ch} (Fig. 3a). At initial stage of step 2, PBTI stress was applied to gate electrode for trap generation. Then, trapped electrons were de-trapped by applying discharge voltage ($V_{discharge}$). After most of trapped electrons are de-trapped by repetitive recovery phase, ΔV_{th} was measured again with increasing t_{ch} at V_{ch} for identifying the change of trap density and trap position under PBTI (Fig. 3b).

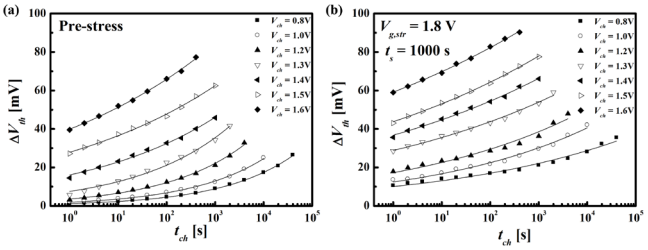

Fig. 3 ΔV_{th} vs. t_{ch} at pre-stress (a) and PBTI stress (b).

The plots of Fig. 3a and Fig. 3b was converted to TSCIS map using the proposed method (Fig. 4). The pre-existing traps related to V_o^{2+} were located at ~0.3 eV below the HfSiON conduction band edge. Once electrons were trapped at pre-existing traps by PBTI stress, the energy level of electron traps was shifted downward by ~0.8 eV due to lattice relaxation. The lattice relaxation such as $V_o^{2+} + e^- \rightarrow V_o^+$ is caused by large polarizability of high-k nMOSFETs [10], so newly generated traps related to V_o^+ were increased and pre-existing traps related to V_o^{2+} were partially decreased under PBTI.

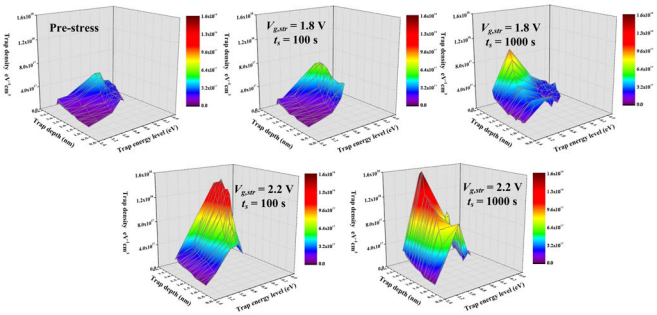

Fig. 4 The oxide rap profile at pre-stress and PBTI stress.

4. Conclusions

A quantitative oxide trap profiling method for both pre-existing and stress-induced oxide traps for HfSiON/SiO_2 dielectric nMOSFETs is proposed. The proposed method uses a TSCIS and measures the stress-induced leakage current (SILC) to determine charge voltage (V_{ch}) and stress voltage ($V_{g,str}$). The extracted trap energy level are shifted downward from 0.323 eV for V_o^{2+} to 0.798 eV for V_o^+ under PBTI. The experimental results indicate that the energy level of electron traps can be shifted downward due to lattice relaxation caused by large polarizability of HfSiON/SiO_2 nMOSFETs under PBTI. Thus, the proposed method is very useful for oxide trap profiling of high-k nMOSFETs which has large polarizability.

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References

[1] K. Xiong, Y. Du, K. Tse, and J. Robertson, J. Appl. Phys. 101 (2) (2007) 024101.

[2] J. Robertson, K. Xiong, and K. Tse, IEEE Conf. ICICDT (2007) 1-4.

[3] I. Hirano, T. Yamaguchi, Y. Nakasaki, K. Sekine, and Y. Mitani, IEEE Trans. Device Mater. Reliab. 9 (2) (2009) 163-170.

[4] M. Sato, T. Aoyama, K. Sekine, T. Yamaguchi, I. Hirano, K. Eguchi, and Y. Tsunashima, Jpn. J. Appl. Phys. 45 (2006) 2949

[5] K. Torii, K. Shiraishi, S. Miyazaki, K. Yamabe, M. Boero, T.Chikyow, K. Yamada, H.Kitajima, and T. Arikado, IEDM Tech. Dig. (2004) 129.

[6] R. Degraeve, M. Cho, B. Govoreanu, B. Kaczer, MB. Zahid, J. Van Houdt, M. Jurczak, and G. Groeseneken, IEEE IEDM tech dig., 775-778.

[7] Y. Liu, A. Shanware, L. Colombo, and R. Dutton, IEEE Electron Device Lett. 27 (6) (2006) 489-491.

[8] DiMaria DJ, Cartier E. J Appl Phys, 78(6) (1995) 3883–3894.