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The Evaluation of PtHfSi/n-Si(100) Schottky Barrier Height by Boron Dopant Segregation with Short Annealing Duration

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Abstract

We investigated the short duration annealing for PtHf-based silicide formation by implementing the dopant segregation (DS) process using boron dopants on n-Si(100). Low SBH for hole of 0.15 eV for PtHfSi/n-Si(100) with *n*-value of 1.07 was obtained after the DS process at 500°C/1 min.

1. Introduction

The Schottky barrier (SB) MOSFET technology is a low-thermal budget process for source and drain (S/D) formation in the gate-first device fabrication [1]. As such, the formation of the metal silicide S/D regions to replace the conventional doped S/D regions is important. Metal silicides such as ytterbium silicide ($YbSi_{2-x}$) for nMOSFET and platinum silicide (PtSi) for pMOSFET are commonly used as S/D regions [2, 3]. To be able to utilize a single silicide material for both n- and pMOSFET for CMOS applications, the dopant segregation (DS) process is used to control the Schottky barrier height (SBH) for electron or hole, respectively. As a result, the CMOS fabrication process would be simpler than using complementary silicides.

In previous reports, the low contact resistivity on PtHfSi/Si(100) with DS process was achieved by using PtHf (5:2) alloy target [4]. Although, the silicidation temperature was as low as 500°C, the annealing duration was long as 20 min.

In this research, the silicidation of PtHf-silicide formation with short annealing duration on n-Si(100) and dopant segregation process to evaluate the SBH was investigated for future CMOS applications.

2. Experimental Procedure

Figure 1 shows the experimental procedure for the SB diode fabrication. First, the n-Si(100) substrates were cleaned by SPM (H_2SO_4:H_2O_2, 4:1) and DHF (HF:H_2O, 1:99). The 100-nm-thick SiO_2 field oxide was formed at 1050°C by wet oxidation process. Next, the 100x100 μm^2 active regions were patterned by photolithography and wet etching. Then, the 30-nm-thick PtHf metal utilizing developed PtHf (5:2) target was deposited using RF magnetron sputtering at room temperature (RT) with 160 W RF power, 2.2 sccm Kr and 0.7 Pa gas pressure. The ion implantation (I/I) of boron (B^+) dopants on PtHf/n-Si(100) samples for the DS process was performed with an ion dose of $1x10^{15}$ cm^{-2} and ion energy of 15 keV. A single step annealing was used for the silicidation and the DS process utilizing RTA at 500°C for 1 min under N_2 ambient. The unreacted PtHf metal was selectively etched by aqua regia solution at 50°C. Finally, the Al back contact was deposited by evaporation. The samples were characterized by J-V, XRD, SEM and 4-point probe measurements. The SBHs were extracted by using the thermionic emission theory.

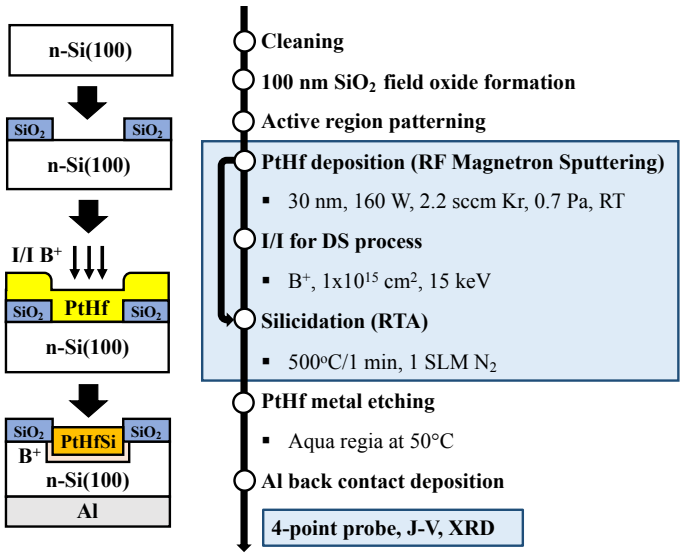

Fig. 1 The SB diode fabrication process.

3. Results and Discussion

Figure 2 shows the XRD patterns of the as-deposited PtHf film and the PtHf-silicide. Since PtSi and HfSi have the same orthorhombic crystal structure, the PtHf-silicide alloy was successfully formed even at short annealing duration of 1 min at 500°C. In this case, the dominant phases obtained after the silicidation process are $Pt_{1-x}Hf_xSi(110)$ and $Pt_{1-x}Hf_xSi(220)$.

Figure 3 shows the J-V characteristics of the PtHfSi/n-Si(100) with and without the DS process. By using the thermionic emission method, the SBH for electron (ϕ_{Bn}) and the ideality factor (n) were extracted. The SBH for hole (ϕ_{Bp}) can be calculated from the equation $\phi_{Bn} + \phi_{Bp} = E_g$ where E_g is the energy bandgap of Si (1.12 eV).

The extracted SBH for hole was reduced from 0.25 eV to 0.15 eV by DS process as shown in Fig. 4. In both cases, low *n*-values of 1.07 and 1.01 were obtained from the PtHfSi/n-Si(100) diodes with and without DS process, respectively.

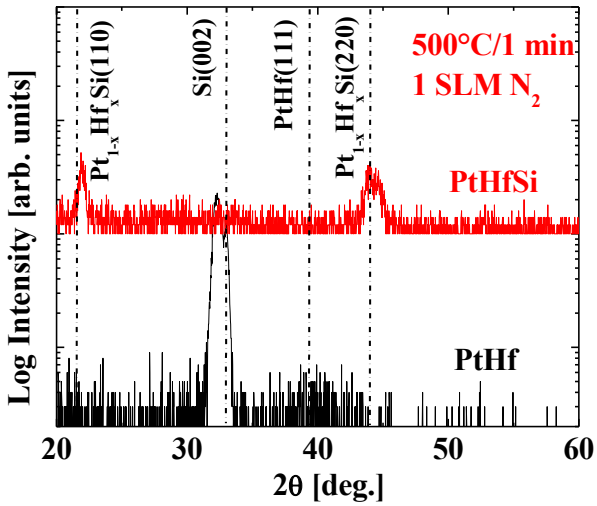

Fig. 2 XRD characteristics of PtHfSi.

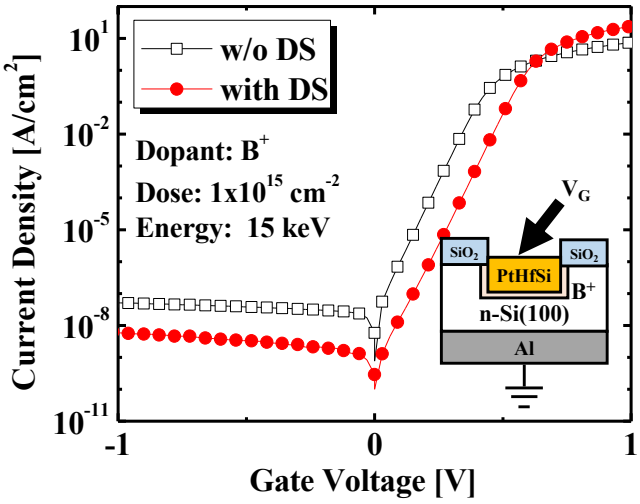

Fig. 3 J-V characteristics of the SB diodes.

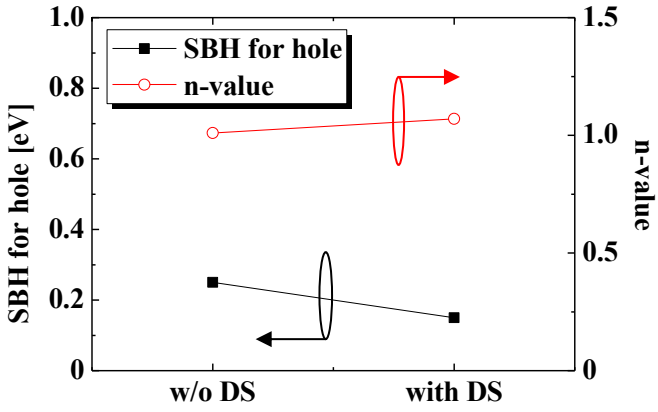

Fig. 4 Extracted SBHs for hole and *n*-values.

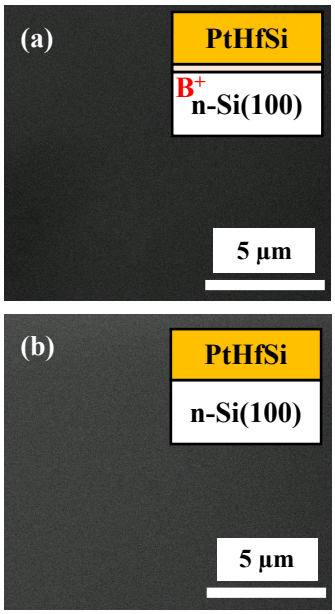

Fig. 5 SEM plan view images of PtHfSi (a) with DS and (b) without DS.

Figure 5 shows the SEM images of the surface morphologies of the PtHfSi on Si(100) with and without the DS process. Smooth surface morphologies were obtained after the DS process and even at the short duration annealing of 1 min. In this case, the short annealing duration is effective in the smooth formation of PtHfSi.

4. Conclusions

The formation of PtHfSi with SBH reduction by DS process was investigated. Low SBH to hole (0.15 eV) was obtained from PtHfSi/n-Si(100) diodes even at short annealing duration of 1 min. In conclusion, the alloying of PtSi with Hf and DS process with 500°C/1 min silicidation annealing are effective in realizing low SBH to hole for CMOS S/D applications.

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