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Effects of Plasma Nitrided Trilayer High-k Gate Dielectric on Electrical Characteristics of FinFET

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Abstract

The stacked high-k gate dielectric on FinFET is rarely seen, although its application on MOSFET was proposed to reduce equivalent oxide thickness. A higher on-current, a higher on/off current ratio, and a smaller subthreshold swing value can be achieved by a TiO_2 inserted trilayer gate dielectric. Since the gate leakage current and reliability characteristics of FinFETs are degraded due to the inserted TiO_2, a HfON inserted at Si/high-k interface is helpful to reduce gate leakage current and improve reliability.

1 Introduction

The high dielectric constant (k) film is widely used as gate oxide in MOSFETs for sub-40 nm technology node. A gate dielectric with a higher k than HfO_2 is desirable to reduce the equivalent oxide thickness (EOT). The dielectric constant of TiO_2 can be up to 80 [1], which is 3.2 times higher than that of HfO_2 [2]. However, it was reported that TiO_2 is apt to diffuse into the channel interface during a high temperature process [3], inducing a large gate leakage current. The leakage current in gate dielectric increases with increasing the contents of TiO_2 [2]. Therefore, a HfO_2 with good thermal stability added at the high-k/channel interface is useful to reduce the diffusion of TiO_2 into the channel. In addition, a HfON formed by HfO_2 treated with NH_3 plasma is proposed to reduce both the EOT and gate leakage current, although its bandgap slightly decreases [4]. In this work, four stacked combinations of HfO_2 and/or TiO_2 as the gate dielectric on electrical characteristics of FinFET were investigated. A HfON formed by HfO_2 treated with NH_3 plasma was also studied to reduce both the EOT and gate leakage current.

2 Experiments

FinFETs were fabricated on 6-inch p-type SOI (100) wafers. The patterns of dummy fins were defined by I-line lithography. Reactive ion etching (RIE) process was performed to form four parallel fins with a fin height of ~40 nm. Then, a trimming was performed on the fins with H_2 plasma for 300 s. Afterwards, the SiO_2 IL was formed in H_2O_2 solution at 75 °C for 10 min. Then, a 4 nm thick HfO_2, a 4 nm thick HfON, a 1.5 nm/2.0 nm/0.5 nm thick $HfO_2/TiO_2/HfO_2$ (HfO_2TiHf), and a 1.5 nm/2.0 nm/0.5 nm thick $HfO_2/TiO_2/HfO_2$ (HfONTiHf) were deposited by an atomic layer deposition (ALD). Afterward, a 100-nm thick TiN film was deposited by sputtering to serve as metal gate. After patterning gate stack, phosphorous implantation (at 40 keV for a dose of 5×10^{15} cm^{-2}) and activation (750 °C for 30 s) were performed on all samples. Passivation and metallization processes were performed, followed by a sintering at 400 °C for 30 min to complete the device fabrication. The sample splits are shown in Table 1.

3 Results and Discussion

Fig. 1 shows transmission electron microscopy (TEM) images of FinFET structure. The height and width of fin channel are about 40 nm and 20 nm, respectively. The thickness of gate dielectric is ~4.0 nm for all samples, which can also be seen from the TEM images.

Table. 1: Sample splits of FinFETs in this work

Sample	HfO_2	HfON	HfO_2TiHf	HfONTiHf
Sinter	400 °C 30 min			
Contact	Al-Si-Cu 200nm			
Activation	RTA 600°C 30s			
Metal gate	TiN 100nm			
High-k	HfO_2 4nm	HfON 4nm	HfO_2+TiO_2+HfO_2 1.5nm+2nm+0.5nm	HfON+TiO_2+HfO_2 1.5nm+2nm+0.5nm
Trimming	300s H_2			
Channel material	Single Crystal-Si			
Substrate	SOI			

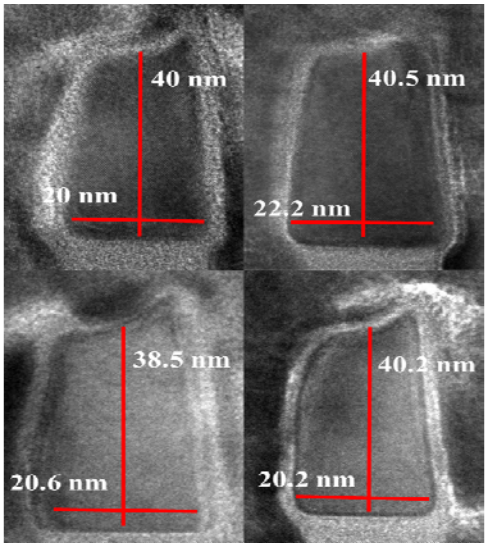

Fig.1: TEM images of FinFETs with (a) HfO_2, (b) HfON, (c) HfO_2TiHf and (d) HfONTiHf gate stacks in this work.

Fig. 2 shows (a) drain current (in log) versus gate voltage (I_d-V_g) and (b) drain current (in linear) versus gate voltage (I_d-V_g) of FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks, respectively. The n-FinFET with stacked high-k HfONTiHf has the highest on current about $3.7x10^{-5}$A. However, the HfON sample has the lowest off current about $2.8x10^{-13}$A, and its on/off current ratio is about 8 orders. The subthreshold swing (S.S.) values of FinFETs were also extracted from the I_d-V_g curves. The S.S. values of devices with HfO_2, HfON, HfO_2TiHf, and HfONTiHf gate dielectric are 72.13, 70.84, 68.93, and 68.92 mV/dec, respectively. Hence, it is found that the S.S. value of FinFET can be reduced with a TiO_2 inserted trilayer high-k gate dielectric stack. Besides, it is clear from Fig. 2(b) that devices with a TiO_2 inserted trilayer high-k gate dielectric have higher drain currents. The improvement can be attributed to the higher dielectric constant of titanium oxide than that of hafnium oxide so that the EOT of TiO_2 inserted gate dielectric stack decreases. In addition, the devices with HfON in high-k gate stack have higher drain currents than those with HfO_2 one, because the k value of HfON is higher than that of HfO_2 one.

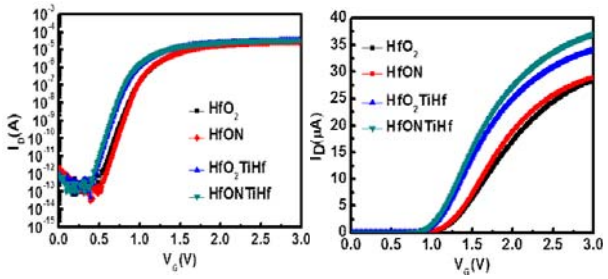

Fig. 2 (a) I_d-V_g in log curves and 2 (b) I_d-V_g in linear curves for FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks.

Fig. 3 shows (a) drain current versus drain voltage (I_d-V_d) and (b) gate leakage current versus gate voltage (J_g-V_g) curves of FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks, respectively. It is found in Fig. 3(a) that the drive current of device with both titanium oxide-inserted gate dielectric stack and HfON are the highest among all samples. The higher drive current can be due to the higher k value. In Fig. 3(b), the gate leakage current of device with hafnium oxide is much lower than that with titanium oxide. The gate leakage current of device with a HfON can be even lower, thanks to the reduced oxygen vacancy by plasma nitirdation. Besides, the high leakage current of the TiO_2 dielectric layer can be due to the small bandgap compared with hafnium oxide. In addition, titanium is easy to diffuse during thermal process, resulting in a leakage path.

Fig. 4 shows (a) threshold voltage shift (V_{th}-shift) and (b) degradation of maximum trans-conductance (Gm,max) versus stress time at a constant voltage stress (E=9 MV/cm) for FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks. The Vt-shift values of devices with TiO_2 stacked gate dielectric are obviously larger. Some defects are formed between the interface of titanium dioxide and hafnium oxide. Consequently, some

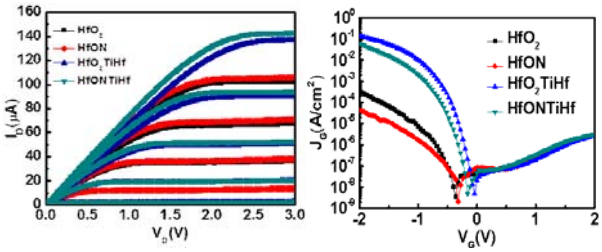

Fig. 3 (a) I_d-V_d curves and 3 (b) J_g-V_g curves for FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks.

hot electrons are trapped in these defects. On the other hand, the Vt-shift values of devices can be reduced by a HfON stacked gate dielectric. The improvement can be again attributed to the reduced oxygen vacancy in HfO_2 by plasma nitirdation. As for the Gm degradation, all devices in this work show the similar results, suggesting the high-k/Si interface is not affected by the high-k gate stack.

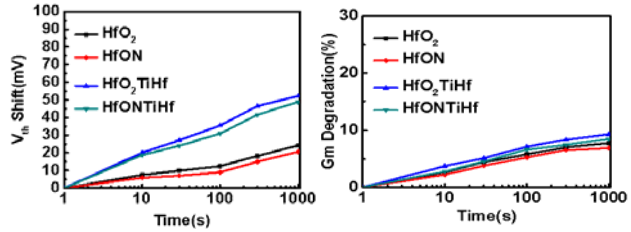

Fig. 4 (a) $V_{th\text{-}shift}$ and (b) $G_{m\text{-}max}$ degradation versus F-N stress time for FinFETs with HfO_2, HfON, HfO_2TiHf and HfONTiHf gate stacks.

4 Conclusions

The stack combinations of HfO_2 and/or TiO_2 as the gate dielectric on electrical characteristics of FinFET were investigated in this work. It is found that FinFET with a TiO_2 stacked gate dielectric has a large drain current, higher on/off current ratio, and a smaller S.S. value. A HfON formed by HfO_2 treated with NH_3 plasma is shown to reduce both the EOT and gate leakage current. Therefore, a titanium oxide-inserted gate dielectric stack and HfON are promising to improve performance of FinFET.

References

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