Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp665-666

Circuit speed oriented device design scheme for double gate hetero tunnel FETs

Koichi Fukuda[1,2], Naoya Nogami[1], Shogo Kunisada[1] and Yasuyuki Miyamoto[1]

[1] Tokyo Institute of Technology
2-12-1 O-okayama, Meguro, Tokyo 152-8552, Japan
[2] National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Umezono, Tsukuba, Ibaraki 305-8567, Japan

Abstract

A device design method of tunnel FET aiming at circuit performance is proposed. The device design takes into consideration the trade-off between quantum effect and gate controllability due to the channel thinning of double gate tunnel FET. The method also takes into consideration the drain current leakage and the effect of gate capacitance. In particular, since gate capacitance behaves differently from CMOS, special consideration is required in device design. In the early stage of the method, we tried design based on intrinsic delay defined by on current and maximum gate capacitance. We evaluated the speed of the ring oscillator and improved the device design method, and proposed a new index called effective delay based on effective current and effective gate capacitance.

1. Introduction

Due to the scaling limit of CMOS technologies, research on new principle transistors are studied actively. The tunnel FET is expected to operate in lower power than CMOS by its steep switching. To enhance the electric field of the band-to-band tunnel region, the authors have succeeded in realizing the GaAsSb / InGaAs double gate hetero tunnel FETs with thin channel below 10 nm experimentally [1]. However, further thinning may cause effective tunnel bandgap widening arising from the formation of the quantum subband. In this paper, these issues are discussed quantitatively by optimizing the component ratio of the source and the channel materials, and by optimizing the device parameters, from the point of the on-current and FET intrinsic delay. Furthermore, dynamic behavior of ring oscillator is evaluated and feed backed to the device design scheme.

2. Simulation method

Fig. 1 shows the device structure of the double gate hetero TFET. The drain concentration is 2~5 × 10^{18} cm^{-3} to suppress the band-to-band leakage current at the drain side. The component ratio considering the lattice matching, channel/drain is In(x)Ga(1-x)As, and source is GaAs(1-0.92x)Sb(0.92x). The semiconductor device simulator ATLAS [2] was used with the nonlocal band-to-band tunneling model. The quantum confinement effect was incorporated by the offsets of the conduction and the valence bands estimated by Poisson-Schrodinger approach. The ring oscillator behavior is evaluated by the device-circuit mixed-mode simulation of ATLAS.

Fig. 2 shows the concept of the effective band gap arising from the quantum confinement effects. The estimated shift of the conduction band ΔE_C and the valence band ΔE_V are incorporated to the band parameters. Fig. 3 is one of the keys of this work which shows the effective band gaps depending on the component x for Ga(x)In(1-x)As, for several channel thicknesses, including the quantum confinement effects.

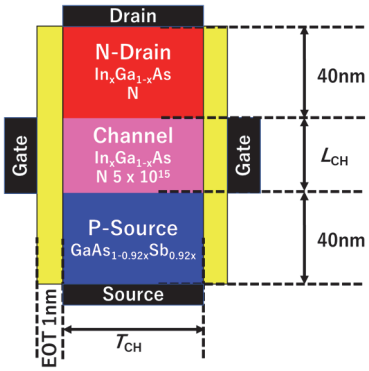

Fig. 1 The TFET structure discussed in this work.

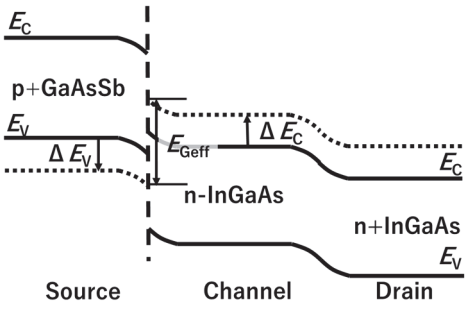

Fig. 2 The concept of the effective band gap arising from the quantum confinement effects.

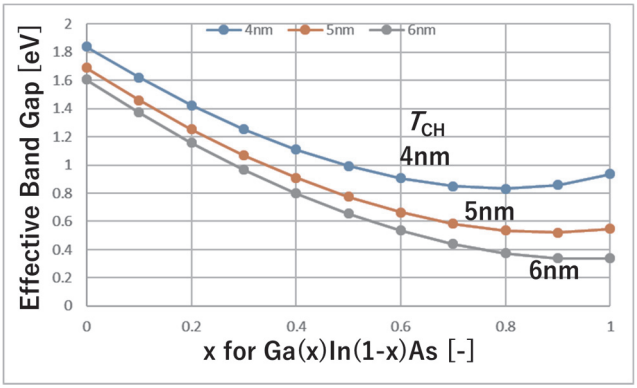

Fig. 3 The effective band gap depending of the component ratio x, for several channel thichnesses T_{CH}.

3. Results and Discussions

Fig. 4 shows I_D-V_{GS} characteristics for 4~6 nm channel thicknesses with each optimum component ratios. The gate length is 35 nm, the source concentration is 3×10^{19} cm^{-3}, and the drain 2×10^{18} cm^{-3}. We fixed the off leakage current I_{OFF} to 10 pA / μm, and the power supply voltage to 0.5 V. The on current I_{ON} is evaluated at the gate over drive of 0.5 V from the off current gate voltage V_{OFF} as shown in Fig. 4.

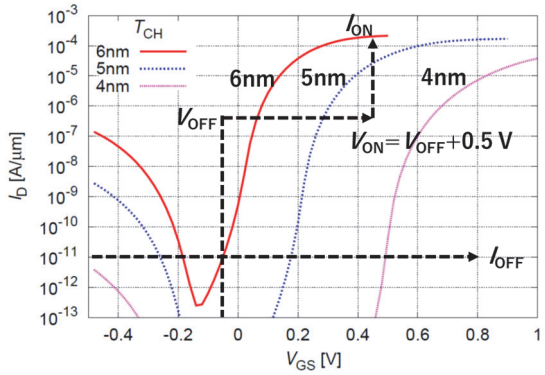

Fig. 4 I_D-V_{GS} characteristics for 4~6nm channel thicknesses.

In the initial stage, the intrinsic delay commonly defined as $C_{GMAX}\times V_{DD}/I_{ON}$ is optimized. Fig. 5 shows the intrinsic delay depending on the channel thicknesses (left) and the source concentrations (right). The minimum delay condition differs from the maximum on current condition, influenced by the contribution of capacitances. The double gate hetero TFETs get merits of the gate capacitances because of lower channel carrier concentrations than the inversion layers of MOSFETs. The intrinsic delay below 1.5 ps is beyond the CMOS target of 2028 low power NMOS with the same I_{OFF} and larger V_{DD} 0.63 V discussed in ITRS 2013.

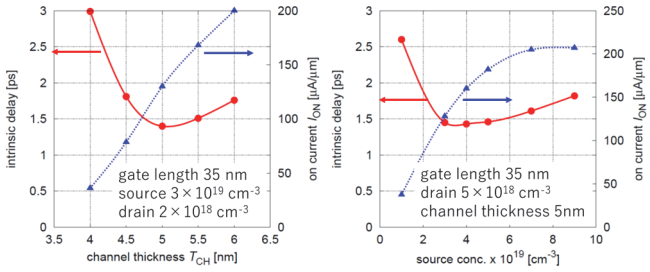

Fig. 5 The intrinsic delays depending on the channel thickness (left) and the source concentration (right).

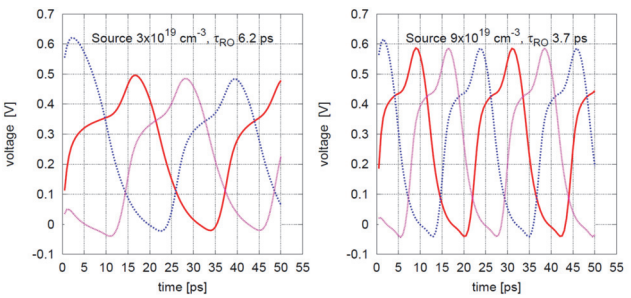

Fig. 6 The 3-stage ring oscillator behaviors by device-circuit mixed-mode simulation for the source 3×10^{19} (left) and 9×10^{19} (right).

Fig. 6 shows the ring oscillator waveforms for 2 cases of source 3×10^{19}, and 9×10^{19} cm^{-3}. Contrary to the intrinsic delay, the ring oscillator is slower for the 3×10^{19} case. This is similar to the MOSFET cases discussed in literatures [3-5].

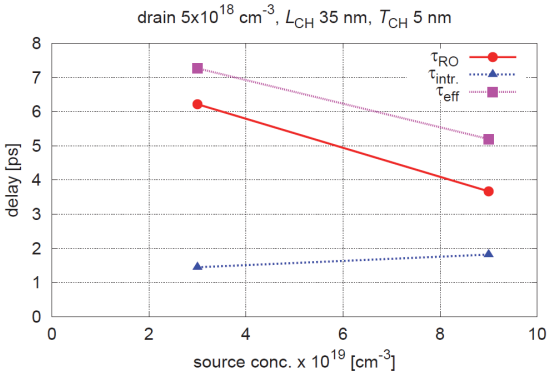

Fig. 7 The ring oscillator delay, the intrinsic delay and the newly defined effective delay for two conditions in Fig. 6.

In Fig. 7, the delay of the ring oscillator, intrinsic delay, and the newly defined effective delay are plotted for the two cases in Fig. 6. The effective delay is defined by $C_{eff}\times V_{DD}/I_{eff}$, where $C_{eff}=(C_H+C_L)/2$ and $I_{eff}=(I_H+I_L)/2$. I_H, I_L and C_H, C_L are drain currents and gate capacitances defined at ($V_{GS}=V_{DD}/2$, $V_{DS}=V_{DD}$) and ($V_{GS}=V_{DD}$, $V_{DS}=V_{DD}/2$) respectively. The defined effective delay explains the tendency of the ring oscillator delay, while the intrinsic delay does not. The proposed effective delay can be evaluated before realizing the circuit, and could be the good device performance index.

3. Conclusions

The device design method of double gate hetero tunnel FET was studied. The method takes into consideration the lattice matching between the GaAsSb source and the InGaAs channel and drain to obtain the optimum component ratio and channel layer thickness. In the optimization process, the increase of the effective band gap due to the quantum confinement effect caused by the channel thinning is considered. In the early stage, optimization was performed based on the intrinsic delay defined by CV over I. In the final stage, we examined the ring oscillator delay and reconsidered the device design method. Finally, the effective delay time is proposed based on the effective drain current and gate capacitance.

References

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