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Improved Electro-Thermal Performance in FinFETs using SOD Technology for 7nm node High Performance Logic Devices

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Abstract

Self-heating effect (SHE) is a serious issue in ultra-down scaled 3-D transistors especially in silicon-on-insulator (SOI) transistors due to lower thermal conductivity SiO_2 buried oxide (BOX) region. However, recently, diamond has become an attractive dielectric material due to its superior thermal conductivity (k_{th} = 2000 $W.m^{-1}.K^{-1}$). In this paper, we designed FinFETs with diamond as BOX region material (i.e. SOD FinFET) and investigated the SHE in comparison with bulk and SOI FinFETs with similar design parameters using 3D TCAD analysis from 14nm to 7nm CMOS technology node. The SOD FinFET shows better heat removal from device active (channel) region by lowering the active region temperature by 17% and 28% compared Bulk and SOI designs respectively. The effective thermal resistance ($R_{th,eff}$) is also lowered by 40% and 54% compared Bulk and SOI FinFETs respectively. This result in lower degradation in drive current for SOD FinFET with efficient active region heat energy removal enabling continued energy-efficient scaling to sub-7nm node. The impact of thermal boundary conditions ($R_{th,GSD}$ and T_A) on transistor performance are also investigated in this work.

1. Introduction

The advances in Si CMOS device technology transformed planar FETs into 3-D transistors and continued energy-efficient scaling for future high-performance (HP) logic devices. However, device self-heating effect (SHE) in confined geometry 3-D MOSFETs, degrades the device performance in terms of increase in active region lattice temperature (T_L). In the case of Bulk and Silicon on Insulator (SOI) FinFETs, gate dielectric (SiO_2) with low thermal conductivity (k_{th}=1.1-1.4 $W.m^{-1}.K^{-1}$) surrounds three sides of the channel. Especially for SOI FinFETs, substrate is also blocked by SiO_2 buried oxide (Buried oxide (BOX); k_{th}=1.4 $W.m^{-1}.K^{-1}$). This results in accumulation of heat energy in drain junction and quasi-neutral region leading to SHE, which degrades both device performance and reliability. Therefore, reducing SHE is a major challenge in sub-10 nm node FinFET designs. Moreover, in bulk FinFETs, with fin width and fin-pitch scaling with technology, the sub-fin region is also getting thinner. This results in reduction of k_{th} (10 times lower than bulk) value for Fin regions with thickness below 10 nm due to enhanced phonon boundary scattering [1]. Therefore, bulk FinFETs are also suffering from SHE with technology down scaling. To continue the more Moore scaling in sub-10nm

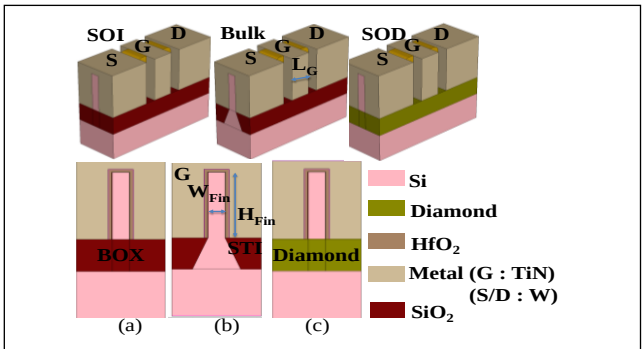

Fig. 1 3-D isometric (top) and 2-D cross-sectional view (bottom) of (a) SOI FinFET (b) Bulk FinFET and (c) SOD FinFET.

with improved electro-thermal immunity, BOX layer should be replaced with another insulator with higher k_{th}. However, nano-crystalline diamond films grown on Si (CVD diamond) have been explored as a lower thermal resistance substrate for Si technology (SOD) due to higher k_{th} of diamond [2], [3] and there have been reports on the enhanced heat removal from the MOSFET active region, fabricated using SOD technology [2], [4]. In this paper, we have investigated the electro-thermal effects in SOD FinFET and compared the results with bulk and SOI FinFET designs.

Table I Physical parameters used in FinFETs design (Units: nm).

L_G	H_{Fin}	W_{Fin}	t_{BOX}	EOT	$N_{S/D}$ (cm^{-3})	N_{ch} (cm^{-3})
20	45	8	20	0.5	$1x10^{21}$	$1x10^{15}$

2. Device Design and Simulation Methodology

In order to investigate device SHEs, we simulated SOD FinFET using Sentaurus TCAD tool with designed parameters (Table I) and compared the results with Bulk and SOI FinFETs (Fig. 1) with same design parameters (Table I). In order to validate our electro-thermal simulations, we have used Boltzmann transport based thermal conductivity model (thickness, doping and temperature dependency on k_{th}) in addition to calibrated carrier transport models in [5].

3. Results and Discussions

For SOD design (Fig. 2(c)), due to the presence of higher k_{th} BOX layer, lower heat energy accumulates in device active region and results in decreasing hot-spot temperature ($T_{L,max}$) to 373K which is 17% and 28% lower than Bulk and SOI FinFETs respectively. This results in lower degradation in drive current (ΔI_{ON}) for SOD FinFET compared to other two FinFET designs (Fig. 3(a)) Therefore, heat mitigation is

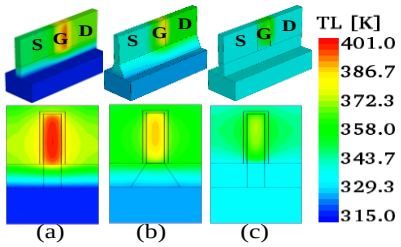

Fig. 2 (top) Simulated lattice temperature profile of 3-D isometric and (bottom) 2-D cross-section at hot-spot location for (a) SOI FinFET (b) Bulk FinFET and (c) SOD FinFET..

better in SOD FinFET compared to both SOI and Bulk FinFET designs. The extracted effective thermal resistance ($R_{th,eff}$) for SOD FinFET is also lowered by 40% and 54% compared to Bulk and SOI FinFETs (Fig. 3(b)) due to its uniform heat spread in device active region (Fig. 2(c)).

However, in FinFETs, major part of heat energy transport through contacts and BEOL metal interconnects. Therefore, thermal boundary conditions (TBC) such as thermal contact resistance for gate, source, and drain ($R_{th,GSD}$) and ambient temperature (T_A) impacts heavily on device $T_{L,max}$. The above analysis is done for fixed TBC of gate, source and drain ($R_{th,GSD}$=$5x10^{-5}$ cm^2KW^{-1}, T_A=300K). But in reality, $R_{th,GSD}$ vary depending on metal lines used in BEOL connec-

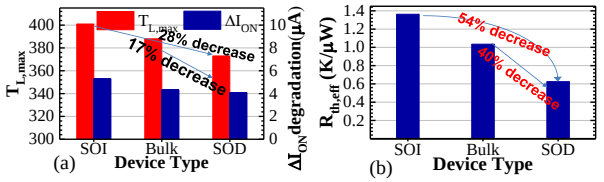

Fig. 3 (a) Hot-spot temperature ($T_{L,max}$) and reduction in drive current (ΔI_{ON}) (b) Device effective thermal resistance for Bulk, SOI and SOD designs.

tion in IC fabrication. The IC ambient temperature (T_A) for the device will also varies depending on the number of adjacent transistors, which are exposed to SHE, which depends on the type of logic operation in the IC. In this paper, we have investigated the impact of $R_{th,GSD}$ and T_A (Fig. 4) and is discussed below.

For decade increase in $R_{th,GSD}$, the raise in $T_{L,max}$ ($\Delta T_{L,max}$) for SOD FinFET is 56 K, which is 8% and 23% lower than Bulk and SOI FinFETs respectively. This result in lower degradation in I_{ON} for SOD FinFET (ΔI_{ON}=1.25μA) compared to SOI (ΔI_{ON}=2.61μA) and Bulk FinFET (ΔI_{ON}=1.41μA) (Fig. 4(a)). It is also observed that the raise in $R_{th,eff}$ for SOD FinFET is only from 0.6 to 0.64 K/μW, which is 92% and 93% lower than Bulk and SOI FinFETs respectively (Fig. 4(b)). From Fig. 4(c) the $T_{L,max}$ of SOD FinFET is low for all T_A values and results in lower degradation in I_{ON} compared to other two designs.

With scaling down (~0.7x) target devices from 14nm to 7nm node, the $T_{L,max}$ for SOI FinFET is further raised by 59% (Fig. 5(a)) and reaching close to Debye temperature limit (Θ_D=640K). However, in SOD FinFET, the $T_{L,max}$ is increased by 35% only, which is far below Θ_D and hence the degradation in drive current is low (50%), compared to SOI (54%) and Bulk FinFETs (92%). This will conclude that with

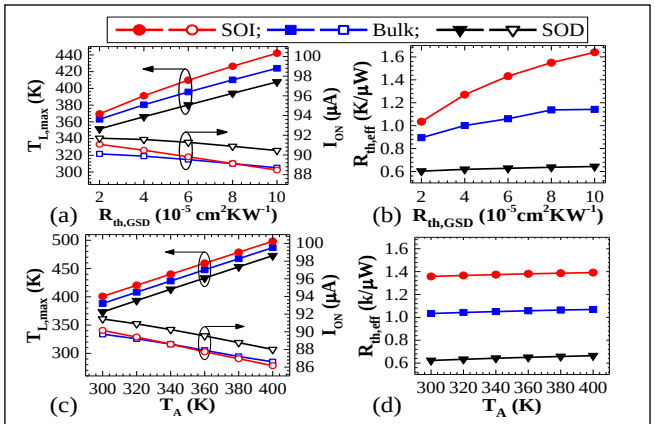

Fig. 4 (a) Hot-spot temperature ($T_{L,max}$) and drive current (I_{ON}) vs $R_{th,GSD}$. (b) Device effective thermal resistance ($R_{th,eff}$) as a function of $R_{th,GSD}$. (c) I_{ON} and $T_{L,max}$ vs T_A, (d) $R_{th,eff}$ vs T_A for Bulk, SOI and SOD designs.

SOD technology, transistors can be aggressively scaled down to sub-7nm node with better heat mitigation, SOD FinFETs are better choice for future HP CMOS logic devices.

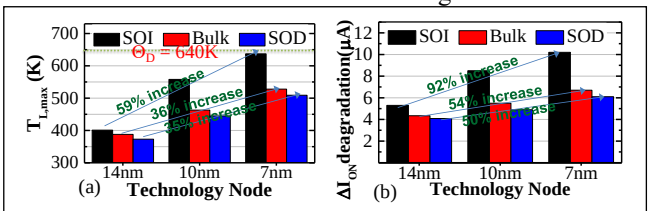

Fig. 5 (a) Hot-spot temperature ($T_{L,max}$) and (b) ΔI_{ON} degradation in drive current for Bulk, SOI and SOD designs with technology scaling from 14nm to 7nm node.

4. Conclusions

In this work, we have numerically investigated SHEs and observed that heat mitigation is better in SOD FinFET, compared to both SOI and Bulk FinFET design due to record high heat conductivity of buried CVD diamond layer in SOD FinFET. For SOD wafer based FinFET designs, lower drive current degradation due to SHE and lower effective device thermal resistance is observed. Finally, we conclude that with SOD technology FinFETs can be aggressively scale down to sub-7nm nodes for HP CMOS logic devices with better heat mitigation.

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