Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp967-968

# Nanostructured High-Performance Thin-Film Transistors Fabricated by Near-Field Nanolithography Strategy

Kairong Huang[1], Zihao Chen[1], Sujuan Hu[1], Jin Wu[1] and Chuan Liu[1]

[1] State Key Lab of Opto-Electronic Materials & Technologies, Guangdong Province Key Lab of Display Material and Technology, School of Electronics and Information Technology,
Sun Yat-Sen University
Guangzhou 510275, China
Phone: +86-136-2225-1273 E-mail: liuchuan5@mail.sysu.edu.cn

**Abstract**

**We develop high-performance oxide TFTs with nanoscale and periodic degenerately doped heterostructures by using a strategy based on near-field nanolithography. These nanostructured TFTs yielded a nearly 20-fold increase in transconductance and apparent device mobility, compared with homogeneous IGZO TFTs. The on–off ratio was higher than $10^9$, with notably enhanced output current and clear scaling effect with channel length. This study shows the viability of programming a variety of nanoscale sub-micron patterns or interfaces to significantly enlarge the scope of research on multi-functional TFTs.**

## 1. Introduction

Conventional Thin-film transistors (TFTs) use continuous, homogeneous, and uniform semiconductors as active layers to implement carrier accumulation and transport. Recently, microstructures have been introduced to TFTs to offer better electrical properties and mechanical flexibility, such as wavy structures, nanogrooves, nanowires, and split structures.[1] Despite the advancements in TFTs with micron-scale microstructures, a general and versatile method to create sub-micron structures and interfaces to facilitate charge transport or induce interfacial effects is still lacking. For practical applications, TFTs yielding a large output current and high device mobility (e.g., over 50 $cm^2V^{-1}s^{-1}$) are desirable to drive high-resolution displays or Virtual Reality with organic light-emitting diodes (OLEDs) or micro-LEDs.

In this study, we successfully developed high-performance nanostructured transistors with degenerate/non-degenerate heterojunctions by a simple but effective near-field photolithographic strategy to produce nanostructures on surfaces covering several square centimeters. By using an array of pristine total-reflective polydimethylsiloxane (PDMS) pyramids or trenches, light beams are diffracted or reflected by slopes until they focus to expose the underlying photoresist, generating sub-wavelength geometries as small as below 100 nm in width. Based on an oxide semiconductor (InGaZnO), the nanostructured TFTs exhibited output current and transconductance nearly 20 times higher than conventional TFT and, thus, a high on–off ratio (> $10^9$).

## 2. Results and discussion

For active layers of the heterojunction, a 50-nm ITO was first deposited by direct-current (DC) sputtering, and was then patterned with sub-micron gaps by photolithography using total reflective PDMS trenches (**Fig. 1a**). In PDMS mask with a periodic array of micro-pyramids or trenches, the normal-incidence light transmitted onto an underlying photoresist surface can take one of three possible paths, as shown in **Fig. 1b**. Normal-incidence ultraviolet (UV) light through the sidewalls is first reflected and then refracted to another pyramid or trench.[2] With multiple refractions and reflections, light is mostly trapped inside the PDMS mask and generates a high-intensity area near the tip. Simultaneously, light through the apexes directly penetrates the substrate and forms high-intensity areas as small as the sizes of the apexes. Consequently, only the photoresist below the apexes is completely exposed, thereby producing periodic sub-wavelength nanostructures. The nanopatterned samples were then deposited on a 70-nm IGZO film through RF sputtering followed by conventional photolithography to define the region of the active layer. After annealing at 350 ℃ for 1 h, the source and drain electrodes consisted of 100-nm-thick Al deposited by ac sputtering through shadow masks.

As shown in **Fig. 2a**, these heterojunction TFTs are typical bottom-gate top-contact structure. The scanning electron microscopy (SEM) image shows that gaps between neighboring ITO strips were 315 nm wide. The subsequent IGZO film filled in the ITO nanogaps, which generated a vertical heterojunction through ITO to build the path of the current between the source and the drain electrodes.

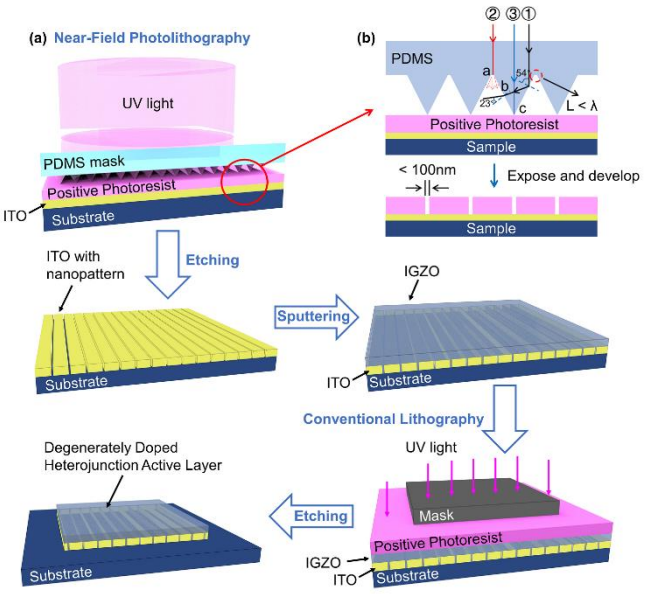


Fig. 1 (a)The fabrication processes of periodic degenerately doped heterostructures active layer. (b)Schematic of near-field photolithography with textured mask.

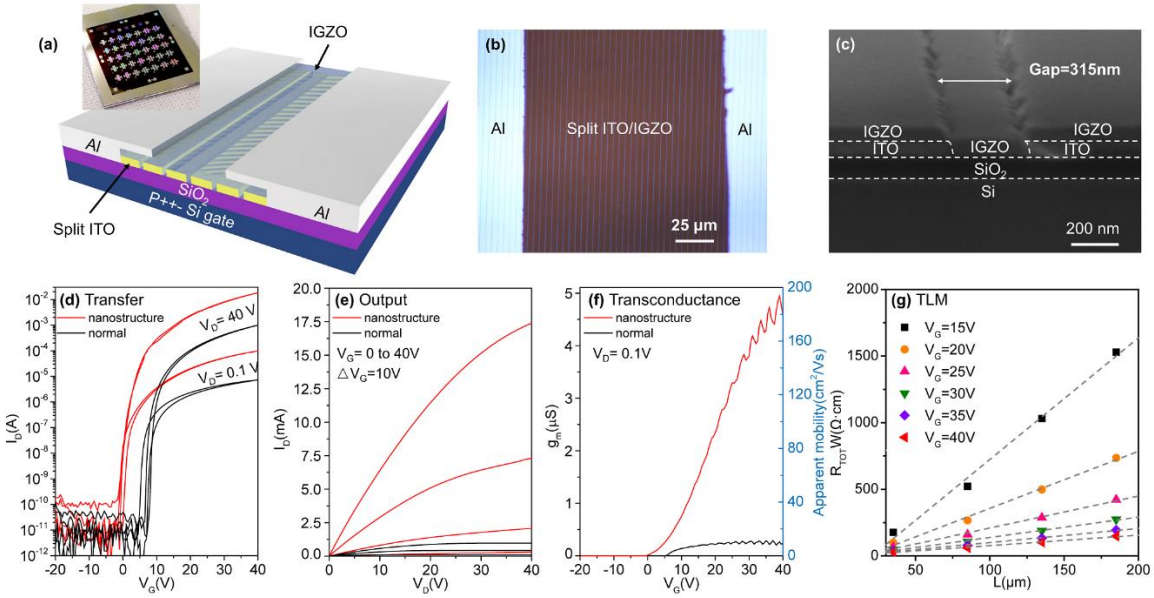


Fig. 2 (a) Schematic and optical images of transistor arrays. (b) Images taken from optical microscope. (c) Cross-sectional SEM image of the heterojunction channel. (d-f) The electrical properties of devices with nanostructured heterojunctions channel (red lines) or normal IGZO TFT (black lines). (g) Width-normalized total resistance of nanostructured heterojunction TFT with $SiO_2$ dielectric layer as a function of channel length $L$. The gate voltage is varied from 15 to 40V in a step of 5V.

The electrical properties of the heterojunction TFTs are shown **Fig. 2d-f**. In both the linear and the saturated transfer scanning, the device exhibited strong gate tunability and high on–off ratio without observable hysteresis during forward and backward scanning. Devices with the proposed method using nanoscale and periodic heterojunctions achieved drain current $I_D$ an order of magnitude higher than and off-current identical to the conventional TFTs with uniform IGZO channel layers, as shown in **Fig. 2d and 2e**. In the saturated regime (gate voltage $V_G$ = 40 V and drain voltage $V_D$ = 40 V), the drain current reached 17.5 mA, 17.5 times higher than that in the conventional IGZO TFT ($I_{Dmax}$ = 0.996 mA). In the linear regime ($V_G$ = 40 V and $V_D$ = 0.1 V), a similarly large enhancement was obtained for $I_D$ and transconductance $g_m = \frac{\partial I_D}{\partial V_G}$. The detailed relations between transconductance and differential apparent mobility with $V_G$ are shown in **Fig. 2g**. Note that these values are not the field-effect mobility of the active layer but the apparent mobility for the device, and can be regarded as the figure of merit for measuring the gate-tunability of conductance and the output current. When using the method of extraction of field-effect device mobility, the linear and saturated device mobilities were 165.8 $cm^2V^{-1}s^{-1}$and 144.2 $cm^2V^{-1}s^{-1}$ (from fitting the slope of $I_D$ and $\sqrt{I_D}$ against $V_G$, from $V_G$ = 25 V to 40 V), respectively, both 17 times higher than those of conventional IGZO TFTs with $\mu_{lin}$ = 9.8 $cm^2V^{-1}s^{-1}$ and $\mu_{sat}$ = 8.5 $cm^2V^{-1}s^{-1}$.

The scaling effect guarantees that TFTs are suitable for different sizes of devices, especially for $L$ smaller than 10 μm. Although previous studies have used high-current oxide transistors by employing nanowires or partial capping layers, the scaling effect has rarely been studied.[3] We investigated the scaling effect of channel length $L$ by using the transmission line method (TLM) in the linear regime.[4] The channel resistance ($R_{CH}$) and contact resistance ($R_C$) can be calculated according to:

$$R_{tot}W = R_C W + \frac{L}{\mu C_i (V_G - V_{TH})} \quad (1)$$

Here, $\mu$, $V_{TH}$, and $C_i$, are the apparent device mobility, threshold voltage, and the capacitance of the gate dielectric per unit area, respectively. We clearly observed the scaling effect as the total resistance $R_{tot}$= $V_D/I_D$ exhibited a good linear relation with $L$ as shown in the **Fig. 2g**. The extracted values of apparent device mobility at $V_G$=40 V were 161.3 $cm^2V^{-1}s^{-1}$, close to the values extracted from the transfer curves as shown above.

## 3. Conclusion

In this study, we proposed nanostructured TFTs fabricated by using a facile, cost-effective, and high-throughput near-field photolithography technology. With nanoscale and periodic degenerate/non-degenerate heterojunctions, nanostructured TFTs exhibited 17.5 times the output current and transconductance than conventional TFT and, thus, a high on–off ratio (> $10^9$) with notably clear scaling effect with channel length. This work can provide a platform for the investigation of interfacial effects at the nanoscale and functions in TFTs.

## References


[1] L. Suhui, S. Jiyeong and J. Jin, Adv. Funct. Mater. **27** (2017) 1604921.

[2] A.M. Bowen, M.J. Motala, J.M. Lucas, S. Gupta, A.J. Baca, A. Mihi, A.P. Alivisatos, P.V. Braun and R.G. Nuzzo, Adv. Funct. Mater. **22** (2012) 2927.

[3] H.-W. Zan, C.-C. Yeh, H.-F. Meng, C.-C. Tsai and L.-H. Chen, Adv. Mater. **24** (2012) 3509.

[4] G. Horowitz, P. Lang, M. Mottaghi and H. Aubin, Adv. Funct. Mater. **14** (2004) 1069.