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Spike Timing Dependent Plasticity Characteristics of Tunnel FET based MONOS Memory for Low Power Neural Network Circuits

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Abstract

We proposed TFET based charge trapping memory to reduce the power consumption of the flash memory based neural network circuits. The current-voltage characteristics of the fabricated TFET based memory cell showed typical characteristics of the charge trapping memory. Then, we measured the STDP characteristics of the fabricated TFET based memory cell. The obtained characteristics reproduce the STDP of a biological synapse. These results indicated that there is a possibility of applying the proposed devices to neural network circuits.

1. Introduction

Neuromorphic computing is one of the promising architectures which can perform complex tasks, such as image recognition. Especially, spiking neural networks (SNNs) have attracted much attention because they can perform cognitive tasks that cannot be readily executed by conventional von Neumann computing [1,2]. A synaptic device is one of the most important components to realize the Hebbian learning in neuromorphic computing. Many kinds of synaptic devices which consist of the non-volatile memory have been studied. However, a two-terminal device, such as a resistive change device, needs an additional switching device. Therefore, some researchers have study flash memory based synaptic devices that have spike timing dependent plasticity (STDP) of a biological synapse, as shown in Fig. 1 [3,4].

On the other hand, a tunnel field effect transistor (TFET) has attracted considerable attention as ultra-low power operating devices. Since a TFET has steep subthreshold slope characteristics owing to the operation based on band-to-band tunneling, it can reduce the operating voltage.

In this study, we fabricated the TFET-based charge trapping memory device as a synaptic device to reduce the power consumption of neural network circuits. Then, we demonstrated that the TFET-based charge trapping memory could reproduce the STDP of a biological synapse.

2. Fabrication of TFET based MONOS memory

Fig. 2 illustrates the TFET-based charge-trapping memory and the process flow. In this study, we used the metal-oxide-nitride-oxide-semiconductor (MONOS) structure as the charge-trapping memory. After the isolation process, the ONO layer and poly-Si were deposited. Then, we formed the gated electrode. After that, the P^+ source and the N^+ drain region were formed. Finally, the metallization process was performed.

Fig. 3 and Fig. 4 show the I_d-V_g and the I_d-V_d characteristics of the fabricated TFET-based MONOS memory device. The I_d-V_g characteristics were measured with the gate voltage from -10 to 10 V and from 10 to -10 V. We obtained typical characteristics of the MONOS memory cell.

3. STDP characteristics

We measured the STDP characteristics of the TFET-based MONOS memory cell using the measurement setup shown in Fig. 5. To evaluate the weight update function, we measured the threshold voltage change and the drain current change produced by rectangular pulses pair. One was impressed on the gate, and the other was impressed on the source. Here, $\Delta\tau$ means the delay time between two rectangular pulses. The width (τ_p) and absolution value of the amplitude ($|V_p|$) were 100 ms and 5 V, respectively. The drain voltage was 0 V during the writing operation.

Fig. 6 shows the measurement results of the STDP characteristics of the fabricated TFET based MONOS memory cell. The obtained characteristics reproduce the STDP of a biological synapse. Therefore, we can use the TFET based MONOS memory as the synaptic device using the threshold voltage instead of the weight coefficient. The high voltage of 10 V was impressed between the gate electrode and the P^- body when two pulses overlapped. This means that high voltage time decrease with an increase in the delay between two pulses. Therefore, the threshold voltage which depends on the trapping charge reduces by an increase of the delay time.

Fig. 7 shows the effect of $\Delta\tau$ on the drain current change. These results indicate that $\Delta\tau$ can control the output current of the MONOS memory cell. These results indicate there is a good possibility of applying the Hebbian learning to the neural network circuits composed by TFET based MONOS memory cell.

4. Conclusions

We proposed the TFET based MONOS memory device to reduce the power consumption of the neural network circuits composed by flash memory. The fabricated devices indicated the STDP characteristics of a biological synapse. These results mean the proposed devices have the potential to be a synaptic device.

Acknowledgments

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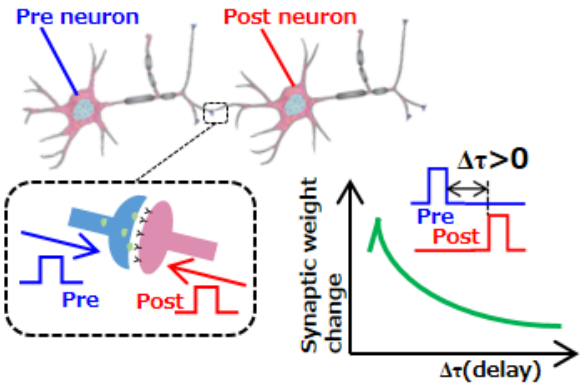

Fig. 1 Schematic illustration of the effect of the spike timing on the synaptic weights.

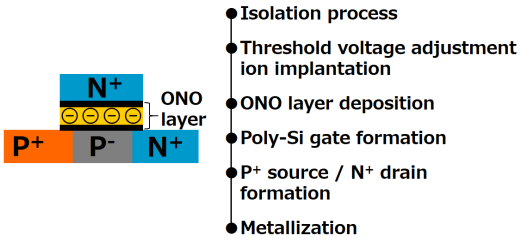

Fig. 2 Cross-sectional image of a Tunnel FET based MONOS memory cell (left) and the process flow (right).

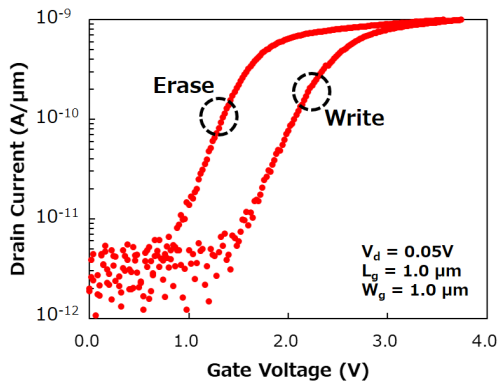

Fig. 3 Id-Vg characteristics of the fabricated MONOS memory cell.

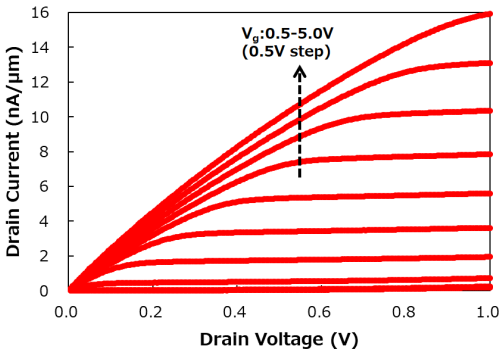

Fig. 4 Id-Vd characteristics of the fabricated MONOS memory cell.

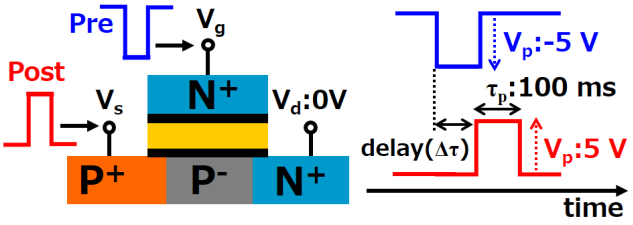

Fig. 5 Measurement setup of STDP characteristics of the fabricated MONOS memory cell.

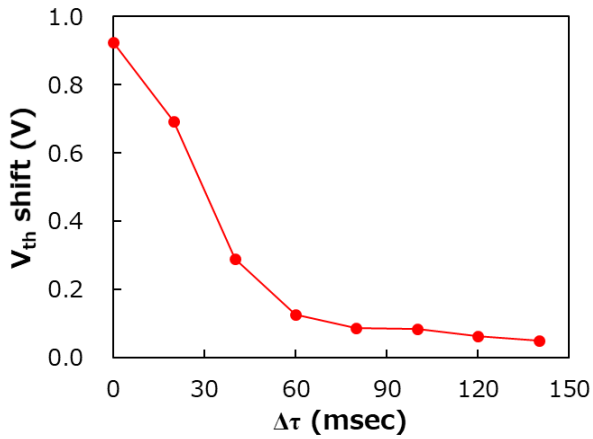

Fig. 6 STDP characteristics of the fabricated MONOS memory cell.

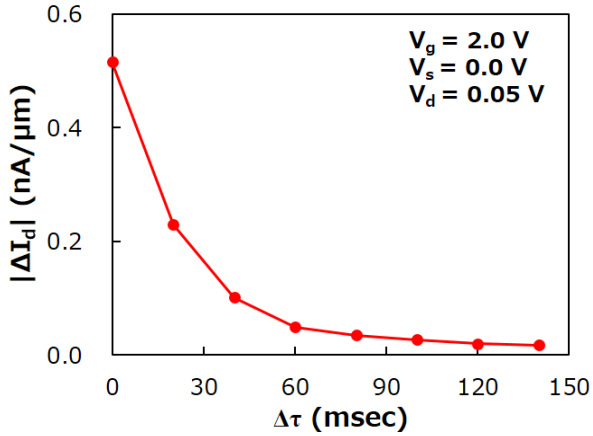

Fig. 7 The effect of the spike timing on the drain current change.