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Synapse Device for Low Voltage Operation and High Conductance Linearity Using Positive Feedback Field Effect Transistor

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Abstract

We propose a positive feedback field effect transistor for low power synapse operation and neural network design method using this device. The proposed FBFET suppresses the sub-threshold current in the low drain voltage situation to enable low power operation. To utilize this feedback device for synapse, we propose a method to modulate the conductance of the device by using the input gate voltage in saw-tooth shaped form and the barrier of the second gate using charge trap nitride. This method ensures a linear synaptic device characteristic at low power. In addition, we measured the FBFET device by making it a CMOS process compatible process. The memory function of the synapse was confirmed by TCAD simulation. At the same time, MAC(Matrix Aggregate Calculator) simulation was performed using the characteristics of this device by Spice.

1. Introduction

The neuromorphic system has been widely used and commercialized in many fields in recent years due to its potential for complex problem solving and low energy consumption. The basic elements of this neuromorphic system are synapse and neuron circuits, in which synapse research is focused on emerging electronic devices such as resistive change memory (RRAM), phase change memory (PCRAM), and FET-based devices[1]. Synapse is responsible for the memory function of the neuromorphic system, that is, the weight quntization. Since the portion occupied by the synapse element in the whole system is overwhelming, it occupies most of the total power, so low power implementation is essential[2]. At the same time, a CMOS compatible process must be possible to fabricate the neuron circuit at the same time, which helps to ensure mass productivity. FET-based devices are CMOS process compatible, which is suitable for the mass production environment. However, in order to secure the linearity of the current modulation, a linear part of the MOSFET is used, which inevitably causes power consumption.

In this work, a positive FBFET (FeedBack Field Effect Transistor) device has a very low subthreshold current and SS (subthreshold swing) value[3-4]. We also proposed a conductance modulation method using this synapse. The memory performance of the device was confirmed by TCAD simulation and MAC(Matrix Aggregate Calculator) simulatino was performed using smartspice.

2. Result and Discussion

Device Structure and measurement results

Fig. 1 is a CMOS compatible fabrication process flow and device structure. The designed FBFET is a p + n-p-n + -doped double gates structure. Gate1 controls the potential barrier of the electron and gate2 controls the potential well size. The well size of the device is controlled by the amount trapped in the oxide / nitride / oxide (ONO) structure between the gate 2 and the channel, and the Vt(Threshold Voltage) of the device is determined according to the trapped amount.

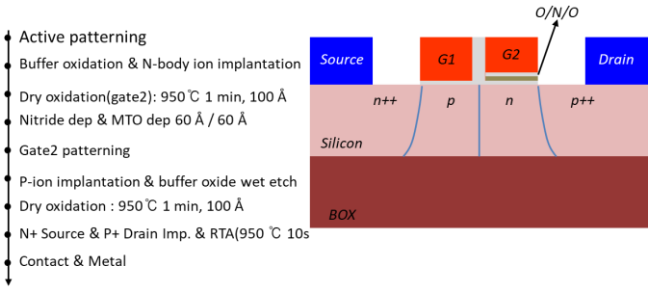

Fig 1. Device structure and and CMOS compatible fabrication process flow

Fig. 2 is the Id-Vg Characteristic measurement value according to the voltage of Gate2. The feedback device is capable of steep switching and almost no current flows when it is not on.

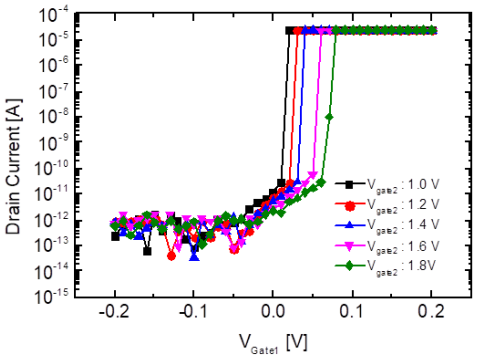

Fig 2. Measured device Id-Vgate1 chracterisitic by Gate2 voltage (Drain Voltage = 1.0V)

It shows that device's operation is modulated according to voltage2. At this time, since the value of Gate2 voltage2

affects the well depending on the amount in the nitrite trap, the value of the voltage2 and the trapped amount are proportional to each other.

Synapse operation and design of system

The synaptic element modulates the amount of current to the current neuron by varying the conductance according to a given weight. To use this feedback device as a synapse, the input signal should be given as a saw-tooth shaped input. When the specific voltage of the Gate1 input exceeds the threshold voltage, the device turns on and a certain amount of current flows by drain voltage. Figure 4 shows that the current is modulated according to Vgate2, the potential well size below gate2, when the input of the saw-tooth shaped is applied.

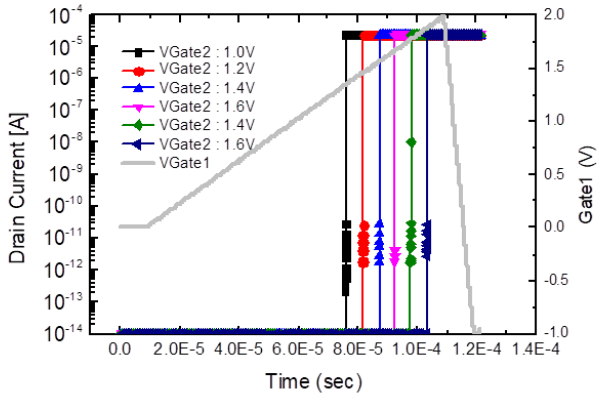

Fig 4. Current modulation by VGate2 with saw-tooth shaped Gate1 input signal

The total amount of charge flowing through the device during a single signal input is summarized in Fig.5. It shows excellent linearity according to Gate2.

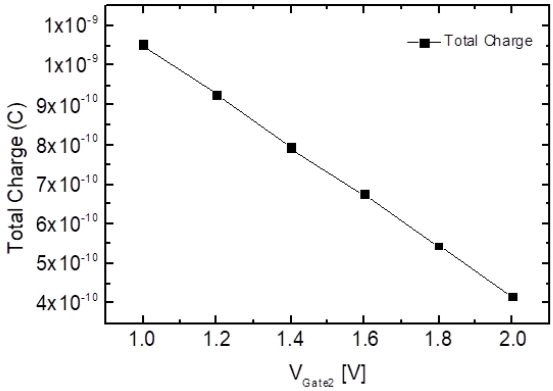

Fig 5. Total charge for 1 input signal by Gate2 voltage

MAC Correlation Simulation

The role of the synapse array is to represent the weight sum by the weight of the input signal and synapse as the membrane potential. In order to perform MAC (Matrix Aggregate Calculator) simulation based on this device, a feedback device was modeled to construct a circuit as shown in Fig. As shown in Figure 7, the R^2 value was 0.95 percent.

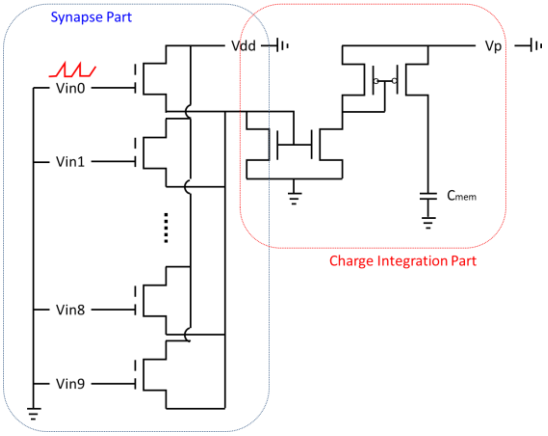

Fig 6. Spice Simulation Circuit for MAC

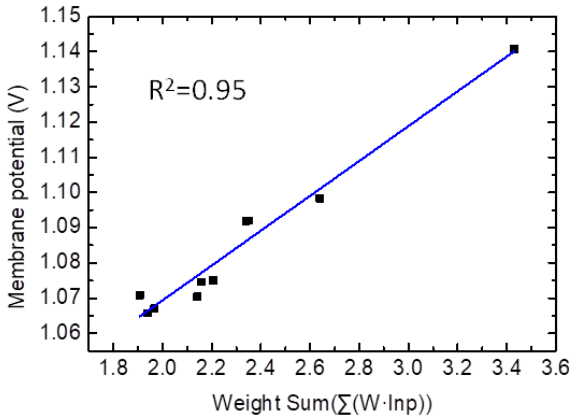

Fig 7. Weight Sum Correlation achieved 0.95

3. Conclusions

We have proposed a method of using synapse device using FBFET low voltage and steep switching operation characteristics. Based on this, we achieved a weigthsum correlation R^2 of 0.95 through MAC spice simulation.

Acknowledgements

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