

Optimal Bias Condition of Dummy WL for Sub-Block Erase Operation in 3D NAND Flash Memory

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Abstract

NAND Flash memory inherently performs erase operation in block unit. The block size of 3D NAND flash memory is enlarged due to an increase of the number of layers. Because of the large size block, which must be erased all at once, it leads to increase program/erase (P / E) cycling in 3D NAND flash memory. To solve this problem, a sub-block erase operation is that dummy word line (DWL) is specified and two blocks are separated and operated based on DWL as a block. However, due to the capacitive coupling effect caused by the DWL, erase operation in the word line (WL) adjacent to the DWL is not normally performed. Therefore, we propose an optimal bias condition for sub-block erase operation using DWL in 3D NAND flash memory.

1. Introduction

NAND flash memory is advantageous in high integration and large capacity storage. It can be used for large-capacity applications because it can minimize cell size. Therefore, Flash memory has been rapidly growing in demand for high-density NAND flash memory devices such as smart phones, tablet PCs, and solid-state drives (SSD) due to its rapid speed, small size, and low power consumption over the past 20 years [1].

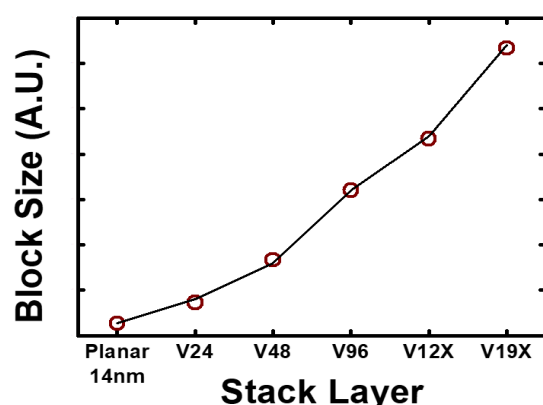


Fig. 1. Block size increase rate with increasing number of 3D NAND flash layers.

In case of 3D NAND flash memory, it is possible to save a lot of data and to increase the integration density as the number of vertical layers increases. However, as shown in Fig. 1 the block size of 3D NAND flash memory is increased, as the number of layers is increased [2-8]. For example, when the 64 layers 3D NAND flash memory is split into two blocks, the string select line (SSL) - 32string - ground select line (GSL) - SSL - 32string - GSL structure is used. Due to the

added size of SSL and GSL, the area overhead increases by more than 10%. Also, as the erase block (EB) size increases, large size blocks are erased all at once, resulting in an increase in P / E cycling. Therefore, there is a need for a technology to realize a small block size that can reduce P / E cycling without increasing the area overhead. Therefore, we propose the optimal voltage for sub-block erase operation using DWL using technology computer-aided design (TCAD) simulation (ATLAS Silvaco™) in 3D NAND flash memory [9].

2. Experimental methods

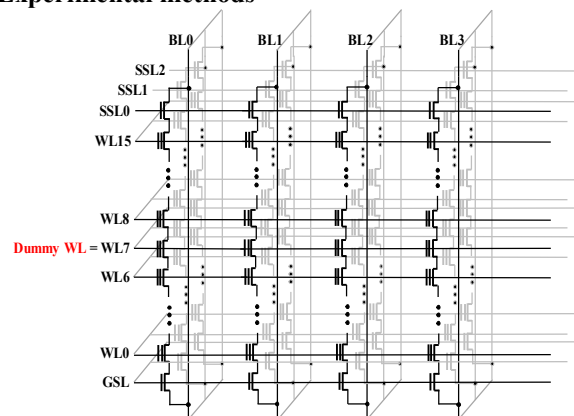


Fig. 2. 3D NAND flash memory string with 16 WL, 3 SSL and 4 BL

Fig. 2 shows the structure of 16 layers 3D NAND flash memory and consists of SSL, WL0 ~ 15 and GSL. SSL and bit line (BL) are shared in 3D NAND flash memory, so the block size can be increased as the number of WL increase. For the experiment, WL7 is used as DWL for sub-block erase operation.

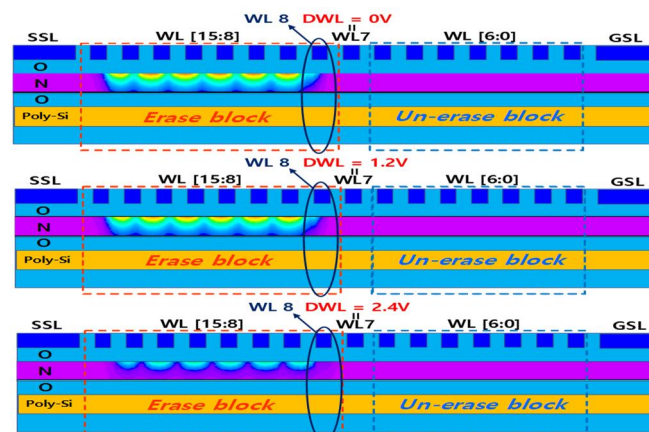


Fig. 3. Simplified vertical diagram of trap hole charge density in 3D NAND flash memory using DWL.

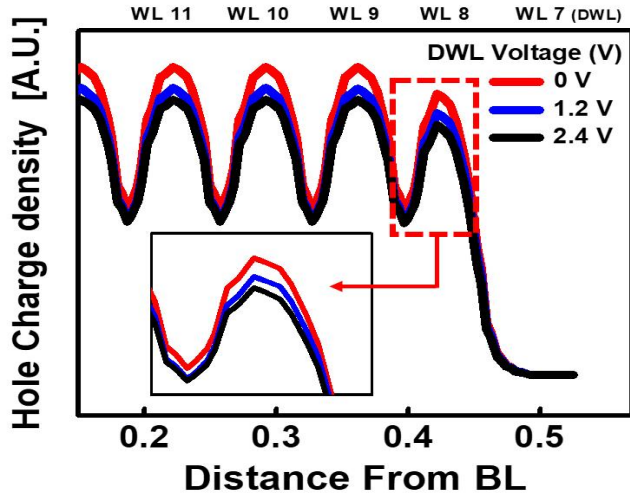


Fig. 4. Trap hole charge density according to DWL voltage.

The experiment of sub-block erase operation using DWL was designated as un-erase block (UB), WL0 ~ 6 and EB, WL8 ~ 15 as shown in Fig. 3. Also, WL7 is used as DWL for sub-block erase operation. Fig. 3 is a vertical diagram of the hole concentration trapped in the nitride according to DWL voltage = 0V, 1.2V, and 2.4V, respectively. As the voltage of DWL increased, the hole concentration trapped in nitride decreased. Fig. 4. shows trap hole capture density according to DWL voltage. The hole concentration of WL8 (WL adjacent to DWL) is lower than that of WL9 ~ 15. In this case, a cell affected by neighboring cells is called a victim cell, and a cell to cell interference (CCI) [10-12]. However, when DWL voltage = 0V, the hole concentration of WL8 is not only the highest but also the hole concentration of WL9 ~ 15 is the highest. It was found that erase was performed most properly when DWL = 0V in 3D NAND flash memory.

	Program	Read	Erase	Erase Verify
SSL	V _{CC}	V _{READ}	Floating	V _{READ}
GSL	0V	V _{READ}	Floating	V _{READ}
Select WL / Un-Select WL	V _{PGM} / V _{PASS}	V _r / V _{READ}	0V / Floating	0V / V _{READ}
Select BL / Un-Select BL	0V / V _{CC}	V _{BL} / 0V	Floating	V _{BL} / 0V
Dummy WL	V _{PASS}	V	0V	V _{READ}
CSL	0V	0V	Floating	0V

Table. 1. The bias condition of sub-block erase operation in 3D NAND flash memory.

Table 1 shows the bias condition for performing the sub-block erase operation. It is similar to the basic operating voltage of planar NAND Flash memory [13]. However, 0V is applied to the DWL in erase operation.

3. Conclusions

In this paper, WL7 is designated as DWL for erase operation in block unit, and a structure in which one block is divided into two blocks based on DWL is confirmed. However, because of the CCI phenomenon, the erase operation was not properly performed. In order to solve this problem, we experimented the optimal bias for sub block erase operation using DWL in 3D NAND flash memory. As a result, erase was performed most properly when DWL = 0V. Sub-block erase technology can reduce the area overhead increase by using only WL without adding GSL and SSL. Also, P / E cycling can be significantly reduced in 3D NAND flash memory.

Acknowledgements

This research was supported by the MOTIE (Ministry of Trade, Industry & Energy (10085645) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device and in part by National Research Foundation of Korea(NRF) funded by the Ministry of Education(2018R1A6A1A03023788) and Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (N000P00008500, The Competency Development Program for Industry Specialist).

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