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Improvement of Hf-based MONOS Nonvolatile Memory Characteristics by Si Surface Atomically Flattening

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Abstract

The effect of Si surface atomically flattening (SAF) on the Hf-based Metal/Oxide/Nitride/Oxide/Si (MONOS) Nonvolatile Memory (NVM) characteristics was investigated. The memory window (MW) of 4.8 V was obtained, and the charge centroid (Z_{eff}) was located at block layer (BL)/charge trapping layer (CTL) interface for the Hf-based MONOS diode with the Si SAF. Furthermore, the MW of 3.2 V was realized for the Hf-based MONOS NVM with improvement of device characteristics by the Si SAF.

1. Introduction

Metal-oxide-nitride-oxide-silicon (MONOS) type memory is a promising candidate to replace the conventional floating-gate (FG) type nonvolatile memory (NVM) [1]. We have reported the excellent electrical characteristics of fully in situ formed Hf-based MONOS NVM, which was able to operate with the input pulse of 6 V/2 ms [2,3].

In this study, the effect of Si surface atomically flattening (SAF) on the Hf-based MONOS NVM was investigated.

2. Experimental Procedure

Figure 1 shows the experimental procedure. The in situ formed Hf-based MONOS NVM was fabricated on p-Si(100) substrate using the typical gate-last process [3]. After the channel stop ion implantation and local oxidation of silicon (LOCOS) isolation, Si(100) SAF process by annealing at 1050°C/60 min in Ar/4%H_2 ambient was carried out [4]. Then, the $HfN_{0.5}/HfO_2/HfN_{1.1}/HfO_2$ (MONO) structure was in situ deposited on p-Si(100) by the electron cyclotron resonance (ECR) plasma sputtering (AFTEX 3400) at room temperature (RT) [3]. The designed thickness of HfO_2 tunneling layer (TL) was 3.2 nm. A 2.1 nm TL was also investigated for the comparison. The $HfN_{1.1}$ charge trapping layer (CTL) thickness was 2.3 nm. The thickness of HfO_2 block layer (BL) and $HfN_{0.5}$ gate electrode was 8 nm each. Then, the post-deposition annealing (PDA) was carried out at 600°C/1 min in N_2. After the contact hole formation and metallization, the post-metallization annealing (PMA) was carried out at 300°C/10 min in N_2/4.9%H_2. The gate length (L) and width (W) of the fabricated device was L/W = 10/90 µm. The inset of Fig. 1 shows the plane-view of the fabricated device.

Figure 2 shows the electrical measurement system overview. The fabricated Hf-based MONOS diodes and NVMs were evaluated by C-V, atomic force microscopy (AFM), I_D-V_D, and I_D-V_G. The operation conditions were set as the program voltage/time (V_{PGM}/t_{PGM}) of 10 V/1 s, the erase voltage/time (V_{ERS}/t_{ERS}) of -10 V/1 s, and V_{DS} of 1.5 V. The charge centroid (Z_{eff}) was extracted utilizing the following equation,

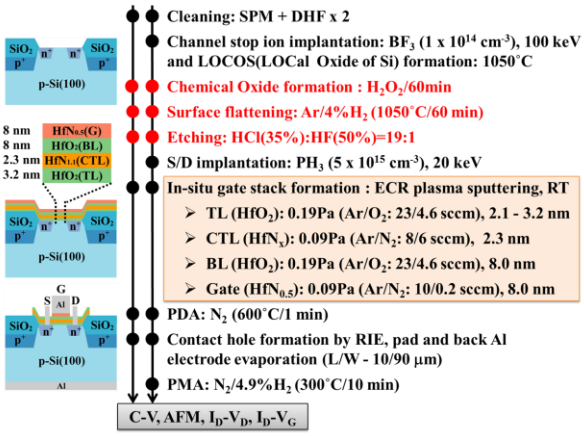

Fig. 1. Fabrication process of Hf-based MONOS NVM with Si SAF.

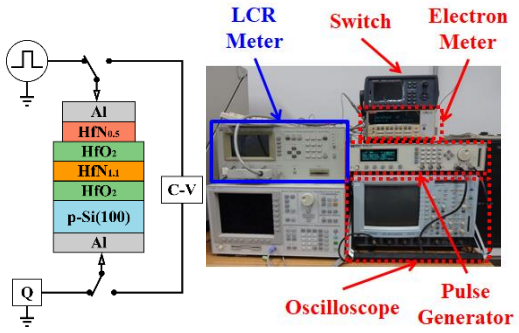

Fig. 2. Electrical measurement system overview.

$$Z_{eff} = \frac{\varepsilon_{OX}\Delta V_{FB}}{\int_{-V_{FB}}^{0} C(V)dV + Q_m} \qquad (1)$$

where Q_m is the measured charge, ε_{ox} is the dielectric constant of HfO_2 BL, and V_{FB} is the flat-band voltage [5, 6]. All measurements were carried out at RT.

3. Results and Discussion

Figure 3 shows the effect of Si SAF on the C-V and memory window (MW) for Hf-based MONOS diodes. The AFM image of atomically flat Si(100) surface is shown as an inset of Fig. 3(a). The charge-injection type hysteresis width was decreased from 40 mV to 10 mV by the Si SAF. As shown in Fig. 3(b), the MW obtained by the program/erase operation was increased from 4.5 V to 4.8 V by the Si SAF when the TL thickness was 3.2 nm. It was more effective for the thinner TL such as 2.1 nm because the interface roughness markedly degraded the retention of the trapped charge with decreasing the TL thickness. Figure 4 shows the extracted Z_{eff} in the $HfN_{1.1}$ CTL region [6]. The distance of Z_{eff} from BL/CTL interface was extracted as 1.3 nm, which is approximately at the center of CTL, for the device without Si SAF. It was found that the Z_{eff} was located at BL/CTL interface region for the device with Si SAF which led to improve the stability of trapped charge in CTL.

The current drivability was improved by Si SAR as shown in the I_D-V_D of Hf-based MONOS NVM (Fig. 5) with the linear mobility of 150 $cm^2/(Vs)$. Figure 6 shows the effect of Si SAF on the I_D-V_G characteristics of Hf-based MONOS NVM. The read operation condition was set as V_D = 1.5 V and V_S = 0 V, respectively. The subthreshold voltage (V_{TH}) was defined as the voltage when the I_D became 10^{-2} A/μm. The extracted MW and ON/OFF ratio were increased from 1.1 V to 3.2 V and 6.5 x10^7 to 2.9 x 10^8, respectively, by the Si SAF.

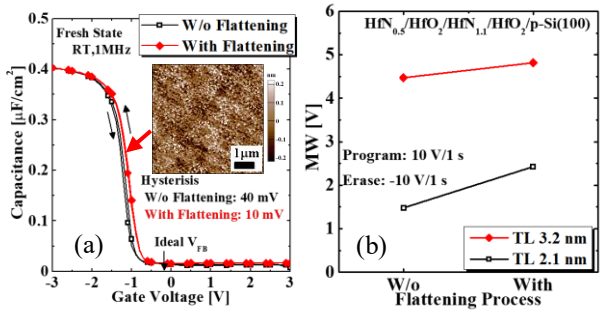

Fig. 3. The effect of Si SAF on (a) C-V and (b) MW of Hf-based MONOS diodes. AFM image of atomically flat Si(100) surface was shown as an inset in Fig. 3(a).

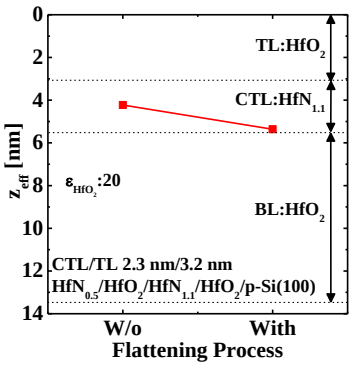

Fig. 4. The effect of Si SAF on Z_{eff}.

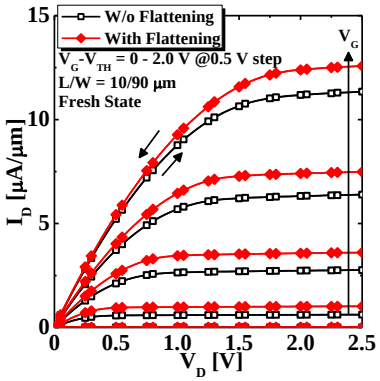

Fig. 5. The effect of Si SAF on I_D-V_D. The L/W was 10/90 μm.

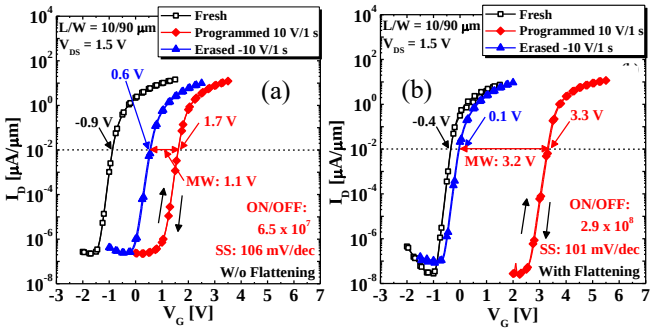

Fig. 6. I_D-V_G of Hf-based MONOS NVM (a) without and (b) with Si SAF. The L/W was 10/90 μm.

4. Conclusions

The effect of Si SAF on the Hf-based MONOS characteristics was investigated. The MW of 4.8 V was obtained, and Z_{eff} was found to be located at BL/CTL interface for the Hf-based MONOS diode with the Si SAF. Furthermore, the MW of 3.2 V was realized for the Hf-based MONOS NVM with improvement of device characteristics by the Si SAF.

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