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Low Power Characteristic of HfO_2 Based RRAM Device with Insertion of Si Film

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Abstract

In this work, TiN/Si/HfO_2/Pt resistive random access memory (RRAM) devices with different thickness of HfO_2 film are fabricated. Stable direct current (DC) 100 cycles under 1μA current compliance and pulse measurement (AC) over 7e4 endurance characteristic are demonstrated. The function of Si film as oxygen scavenge is proposed and characterized with electrical measurement. Compared with the TiN/HfO_2/Pt device, the formation of interfacial layer (IL) between Si film and HfO_2 layer avoids current overshoot, contributing to low power characteristic. Once the deposited HfO_2 film is smaller than 5nm, the soft-breakdown occurs in the whole IL, and the device operation current is up to 1mA.

1. Introduction

As one of the most promising non-volatile memories, RRAM exhibits excellent performances, such as simple structure, low cost, high speed and compatible with CMOS technology [1]. However, most of them suffer high power consumption. Therefore, further development requires small operation current and strong reliability, which however is still a challenge. Cheng C H [2] uses GeO_x layer as hopping layer to limit current, but the Ge material is not compatible with CMOS technology. Govoreanu B[3] uses TiO_2 and Si layer to achieve non-filamentary and low power characteristic, but the TiO_2 film has complex phases and it is difficult to control the quality of TiO_2 film during film deposition, which brings instability during device fabrication. Strachan J P[4] achives <1pJ resistive switching energy, but the ratio of HRS/LRS is just 2, which is not enough to identify two different states.

In this work, we use HfO_2 as resistive switching layer and Si as oxygen scavenge layer to restrain the overshoot effect [5] and fabricate the RRAM device with low power characteristic. The ratio between two states is close to 10. The electrical characteristics of devices are measured with Agilent B1500A, and 81160A.

2. Experiment

The structure diagram of TiN/Si/HfO_2/Pt RRAM device and the corresponding process flow are shown in Fig. 1. The Pt bottom electrode (BE) was prepared by DC sputtering on the Si/SiO_2/Ti substrate. After that, the HfO_2 layer was deposited by atomic layer deposition (ALD) technique, and the Si film was deposited by radio frequency (RF) sputtering. Next, TiN top electrode (TE) was fabricated with DC sputtering. Finally, the square shape TiN/Si/HfO_2/Pt RRAM device was formed by photo-lithography and etching process.

The TE and BE were connected with signal and ground respectively. For the DC measurement, +4V and -3V voltage sweep was applied on the device with 1μA current compliance during set process. Fig. 2(a) showed the 1st, 50th and 100th I-V curves during 100 DC cycles. For the device-to-device distribution, 10 devices were selected randomly, and the corresponding I-V curves were shown in Fig. 2(b). Fig. 2(c) showed the I-V curve of the 50μm*50μm device, the LRS and HRS were similar with the device of 100μm*100μm area. For the pulse measurement, the endurance characteristic over 7e4 cycles with 100ns pulse, 2.2V set voltage and -2.6V reset voltage was achieved with verify scheme[6].

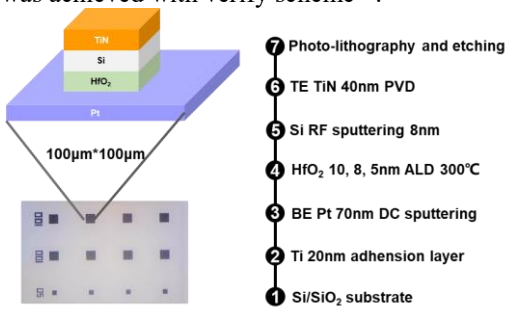

Fig. 1 The device structure and the corresponding process flow of TiN/Si/HfO_2/Pt RRAM device.

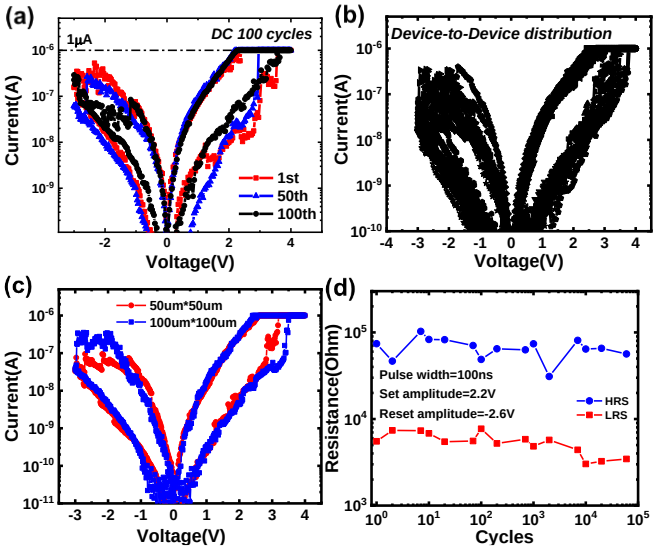

Fig. 2(a) DC measurement for 100 cycles. (b) The device-to-device distribution for 10 devices selected randomly. (c) The I-V curve of 50μm*50μm device and 100μm*100μm device. (d) The endurance characteristic during pulse measurement.

3. Results and discussion

To explore the underlying resistive switching mechanism, the control experiments are carried out. The device with single layer 8nm Si film and 10nm HfO_2 film are fabricated

respectively. The device performances are shown in the Fig. 3. The deposited Si film has low resistivity and the I-V relationship is almost linear. The operation current of the RRAM device with single layer HfO_2 film is up to 1mA. For the device with Si/ HfO_2 double layers, the RRAM can achieve resistive switching process successfully under 1μA current compliance, which is featured with low power characteristic.

For the RRAM device with double layers, changing the thickness of HfO_2 film with 5nm, 8nm and 10nm, the various devices perform differently during forming process, shown as Fig.4. The thicker the HfO_2 film, the smaller the leakage current for the fresh devices. Moreover, the RRAM device with 8nm and 10nm HfO_2 film can achieve the resistive switching process under 1μA, but when the HfO_2 thickness decreases to 5nm, the current is up to 1mA. Besides, after the forming process, the current of device with thick HfO_2 film is approximately equal to the leakage current of the device with thin HfO_2 film.

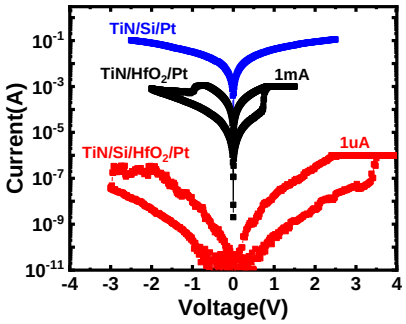

Fig. 3 The I-V curves of three different structures

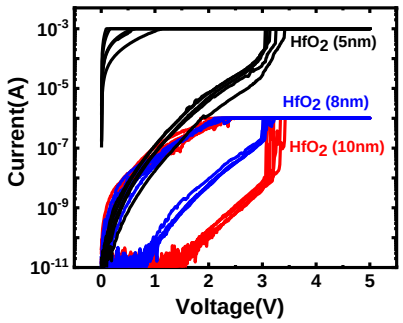

Fig. 4 The forming process of the TiN/Si/HfO_2/Pt devices with different thickness of HfO_2 film

Based on the electrical measurement, the proposed resistive switching mechanism is shown in Fig. 5. The Si film acts as the oxygen scavenge layer and absorbs oxygen ions from HfO_2 layer, causing the formation of non-stoichiometric HfO_x and SiO_x layers. When the thickness of HfO_2 film is over 5nm, there still exits stoichiometric HfO_2 layer, the formation and rupture of the filament mostly occurs in the HfO_2 layer, the interfacial layer (IL) doesn't experience breakdown during forming and set process. The IL acts as the limiting layer to avoid the current overshoot, which contributes to low operation current. When the thickness of HfO_2 film is smaller than 5nm, there is almost no HfO_2 with all IL. The conductive filament is formed in the IL connecting TE and BE, no low power characteristic is observed. To provide evidence further for the proposed resistive switching mechanism. Fig. 6 shows the two-step forming process. After applying the 1st forming voltage, continuing applying more voltage, the 2nd breakdown occurs and the device enters high operation current state. The value of LRS is similar with the device with 5nm HfO_2 layer.

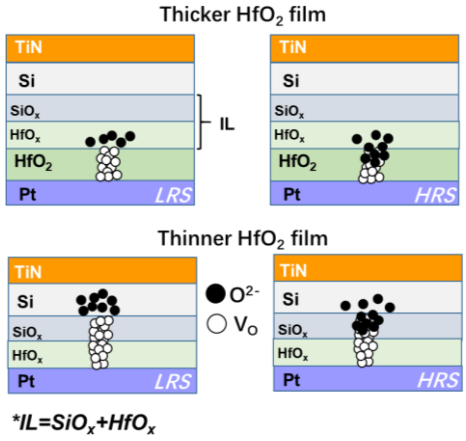

Fig. 5 The schematic graph of the corresponding resistive switching mechanism.

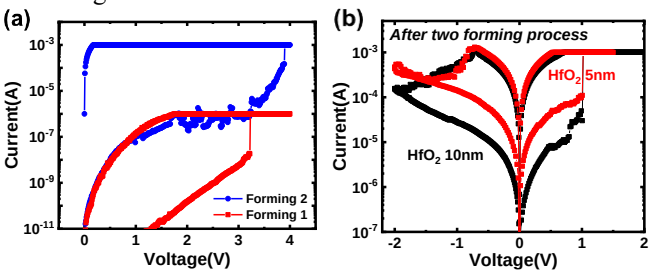

Fig. 6(a) Two-step forming process in the double layer RRAM device with 10nm HfO_2 film. (b) The I-V curve of the TiN/Si/HfO_2(5nm)/Pt device and the TiN/Si/HfO_2(10nm)/Pt device after two-step forming process.

3. Conclusions

The TiN/Si/HfO_2/Pt devices show low power characteristic with the thickness of HfO_2 film not less than 5nm. The resistive switching process occurs in the stoichiometric HfO_2 layer and the non-stoichiometric interfacial layer acts as current limiting layer, which contributes to the low operation current.

Acknowledgements

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