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Physics in HRS-LRS Switching in Vacancy Modulated Conductive Oxide (VMCO) Memories

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Abstract

Vacancy modulated conductive oxide (VMCO) memory is greatly expected as a next generation non-volatile memory. However, the switching mechanism of VMCO memory is still unclear. In this work, we propose a new switching mechanism which can comprehensively reproduce experiments related to VMCO memories. Moreover, we discuss the origin of high on-off switching ratio.

1. Introduction

In recent years, resistive switching memories (ReRAMs) has been attracting considerable attention because of the low power consumption and high speed operation. However, conventional ReRAMs form conductive filaments which function as current paths in the oxide film [Fig. 1]. Therefore, they do not have area dependence in current value, and are not suitable for next generation high density memories. However, vacancy modulated conductive oxide (VMCO) memories, in which the current value depends on the area of the device, have been reported and are now attracting a lot of attention for future high density memories [1].

VMCO memories are ReRAMs in which the insulator is anatase type TiO_2, and the electrodes are TiN and a-Si [Fig. 2]. The most significant features of VMCO memories are the area dependency of the current value as shown in Fig. 3. Therefore, since VMCO memories are suitable for scaling, they are greatly expected as next generation high density nonvolatile memories. Regarding its switching mechanism, it is already considered that oxygen vacancies (Vo) are widely distributed in oxide film as current paths, and when we use rutile type TiO_2 as an insulator, VMCO memories do not work properly. However, the conventional Vo drift model shown in Fig. 4 in which Vo drift by applying voltage is the origin of HRS-LRS switching [1], cannot explain why VMCO behavior appears only in anatase type TiO_2.

In our previous work, we proposed a new switching model in which interface reaction governs the HRS-LRS switching in VMCO memories [3] [Fig.5, Fig.6]. In this work, we explain why rutile type TiO_2 does not reveal VMCO characteristics. Moreover, we also discuss high on-off switching ratio of VMCO memories.

2. Our proposed switching model

First, we explain our switching model for VMCO model in our previous work [3]. We focused on the Vo formation reaction as shown in eq. (1) near TiO_2/a-Si interface.

$$TiO_2 + Si \rightleftarrows TiO_2(2Vo) + SiO_2 \quad (1)$$

In short, if there are Vos near the interface, a low resistance state (LRS) would occur, and if there are no Vos near the interface, a high resistance state (HRS) occur [Fig 5].

Our first principles results show that formation energies of Vo in anatase type TiO_2 and SiO_2 are 4.41eV and -8.42eV, respectively. It means that the reaction in eq. (1) gives 0.4eV energy loss. According to the band diagrams of anatase type TiO_2 with Vo and Si in Fig. 6(a), however, the electrons which occupy the Vo level transfer to Si, resulting in energy gain. This energy gain exceeds the energy loss in Vo formation reactions. Hence, the Vo formation reaction occur and LRS is more stable. Moreover, when positive voltage is applied, energy gain in electron transfer decrease and HRS is more stable [Fig. 6(b)]. According to the above discussion, it is possible to control the formation and disappearance of Vo by applying a voltage near the TiO_2/a-Si interface, and HRS and LRS can be switched in VMCO memories. This can naturally explain the experimental behavior of VMCO memories.,

3. Discussion

First, we discuss the reason why VMCO memories do not work properly when rutile type TiO_2 is used as oxide film. As the calculation results, we found that 0.22eV energy gain occurs in the Vo formation reaction. Therefore, the Vo formation reaction is spontaneous without considering electron transfer. In other words, the Vo formation reaction proceeds regardless of voltage application and LRS is always more stable [Fig.7(b)]. Hence, LRS and HRS cannot be switched in the case of rutile type TiO_2 and it is considered that VMCO memories does not work properly. As discussed above, our proposed model can naturally explain why VMCO memories with rutile TiO_2 do not work, although conventional Vo drift model cannot explain it [Fig.8].

Next, we discuss the on-off switching ratio of VMCO memories. In our proposed model, LRS and HRS are switched by controlling the formation and disappearance of Vo in TiO_2 near TiO_2/a-Si interface. However, if the thickness of the layer that Vo is controlled is too thin, electrons tunnel even if there is no Vo. Therefore, the thickness of this layer is critically important for on-off switching ratio. This thickness can be estimated by considering interface dipole as shown in Fig. 9, and it is estimated as 2.65nm when Vo density near interface is $6.0 \times 10^{20}\mathrm{cm}^{-3}$ by using the equation given in Fig.10. From these results, electrons do not tunnel easily in HRS. Therefore, in our proposed switching model of VMCO memories, high on-off switching ratio is ensured.

4. Conclusion

In this work, we proposed the switching model of VMCO memories by considering the reaction near TiO_2/a-Si interface. In the same way, we also clarified the reason why VMCO memories do not work in the case of rutile type TiO_2 insulator. Moreover, we also confirmed that the high on-off ratio is ensured in VMCO memories described by our model.

References

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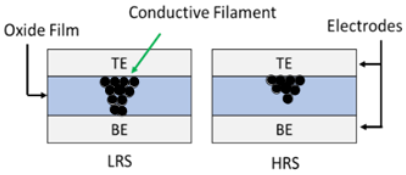

Fig. 1. The switching mechanism of a conventional ReRAM. The ReRAM exhibits LRS when a conductive filament is formed and exhibits HRS when the conductive filament is broken.

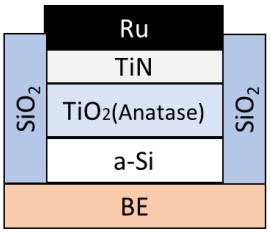

Fig. 2. Schematic illustration of VMCO memory [3].

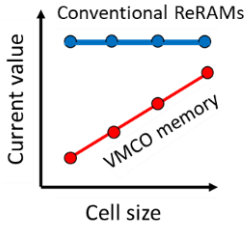

Fig. 3. The area dependency of current value. The current value of VMCO memory decreases when its cell size decreases [3].

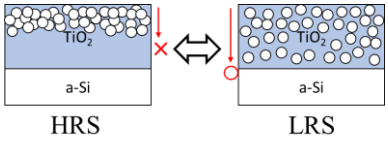

Fig. 4. The drift model for VMCO memories. Vos drift by applying a voltage. The red arrows signify current. This model cannot explain the reason why VMCO memories do not work when rutile type TiO_2 is used.

Fig. 5. Our switching model for VMCO memories. The Vo formation reaction near the interface is controlled by applying a voltage. The red arrows signify current [3].

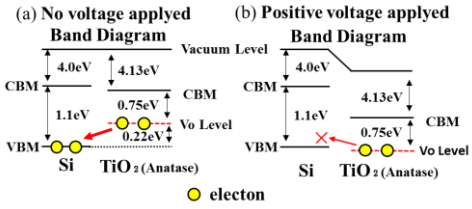

Fig. 6. (a) Band diagrams of Si and anatase type TiO_2 with Vos [4]. (b) Band diagrams of Si and anatase type TiO_2 with Vos under positive voltage. The energy gain in electron transfer decreases by applying a voltage [3].

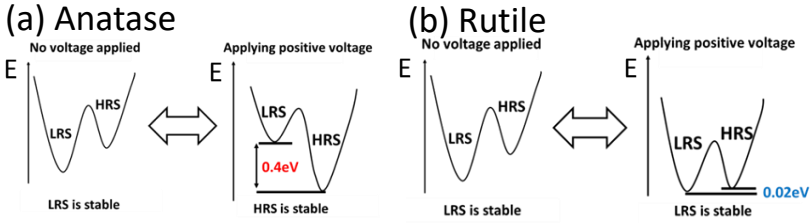

Fig. 7. (a) The behavior of VMCO memories by voltage application in the case of using anatase type TiO_2. (b) The behavior of VMCO memories by voltage application in the case of using rutile type TiO_2. While the stable state can be switched when anatase type TiO_2 is used, the stable state can not be switched when rutile type TiO_2 is used.

Switching model	Anatase type	Rutile type
Vo drift model	○	×
Present model	○	○

Fig. 8. Comparison of Vo drift model and present model. Present model can also explain why VMCO memories do not work when Rutile type TiO_2 is used.

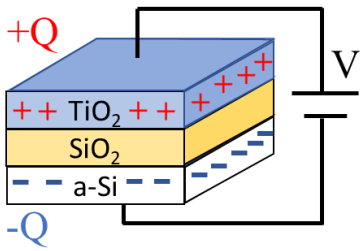

Fig. 9. A state of interface dipole. Near TiO_2/a-Si interface, TiO_2 is positively charged and a-Si is negatively charged. It is regarded as a parallel plate capacitor.

$$\sigma^2 - \frac{2W\varepsilon\rho}{e^2 l} = 0$$

$\sigma(/\mathrm{cm}^2)$: density of Vo

Parameter	Value
W : energy stored in capacitor	0.12eV
ε : dielectric constant of SiO_2	3.36×10^{-11}F/m
ρ : (100) surface density of Si	$6.8 \times 10^{14}/\mathrm{cm}^2$
e : elementary charge	1.6×10^{-19}C
l : 1ML thickness of (100) Si layer	1.36Å

Fig. 10. The equation for finding number of Vo and value of each parameter.