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Current Monitor Circuit with Cascode Amplifier Using Crystalline IGZO FETs Compatible with Low-Voltage Input to Detect Micro Short-Circuit in Lithium Ion Battery

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Abstract

We have fabricated a current monitor circuit (CMC) using crystalline indium-gallium-zinc oxide semiconductor field-effect transistors (IGZO-FETs) to detect micro short-circuit in a lithium ion battery. This work shows the construction of a cascode amplifier composed of only NMOS FETs and the compatibility with input of low voltages.

1. Introduction

Lithium ion batteries adopted in a variety of electronic devices have boosted convenience for many users. Meanwhile, there are reports of fire accidents one of the supposed causes of which is micro short-circuit (also referred to as internal short-circuit or soft short-circuit) of lithium ion batteries [1]. The micro short-circuit is a failure mode where short-circuit occurs between a positive electrode and a negative electrode, which is caused by growing a lithium metal plated on the negative electrode to reach the positive electrode. The micro short-circuit during charging causes a fluctuation in charging voltage or charging current.

Research on a method for detecting micro short-circuit has been currently promoted, and there is a report of a comparator that detects a fluctuation in charging voltage due to micro short-circuit [2]. The report indicates an NMOS comparator composed of only n-type crystalline indium–gallium–zinc oxide semiconductor field-effect transistors (IGZO-FETs). Such a comparator is constructed from analog circuits such as a sample-and-hold (S/H) circuit and a current-load comparator. The S/H circuit enables long-term voltage retention by utilizing low leakage current of IGZO-FETs. It is difficult to adopt this technology to MRAM and ReRAM. Such a low leakage current is expected to be utilized for a memory module and other items related to IGZO-FETs [3–6].

This work reports a current monitor circuit (CMC) that measures charge current to detect micro short-circuit. The CMC is constructed with an integrator using only IGZO-FETs, like the above-mentioned comparator [2]. Specifically, technology for a high amplification factor to increase signal detection accuracy, technology for detecting GND-level signals, and evaluation results of the CMC are shown in this report.

2. Characteristic of the IGZO-FETs

Figure 1 shows V_g–I_d curves of IGZO-FETs (W/L = 0.36 μm/0.36 μm). The off-state current of the IGZO-FETs is below the measurement limit. The threshold voltage of the IGZO-FETs greatly depends on the back-gate electrode.

3. Design of the CMC

Figure 2 shows a V–F converter as a CMC in this work. The V–F converter has been generally used as CMCs for batteries [7]. The current from the battery flows into a shunt resistor, and some amount of the current is integrated in an integrator. A hysteresis comparator constructed with a comparator and NAND switches on and off states of input switches SW1 and SW2 when an output of the integrator is higher than V_{REFH} or less than V_{REFL}. A frequency for the switching varies in accordance with the current flowing through the battery.

Figure 3 shows an amplifier for the integrator in this work. The amplifier has an offset cancellation function. An offset voltage is retained at capacitors Cm1 and Cm2 while V_{REF1} is directly input to a transconductance amplifier Gm on the first stage, so that the offset is cancelled [8]. For an additional offset cancellation function, choppers are provided for an input and an output [9].

The above-mentioned amplifier [2] is a current-load amplifier combined with an S/H circuit with a higher amplification factor than a diode-connected or resistance-load amplifier. However, the amplification factor of such an amplifier is not sufficient for the integrator of the CMC. Figure 4 shows a trasnconductor amplifier Gm in this work. M1 serving as a current load is cascode-connected to M3. The S/H circuit retains V_{BIAS} and V_{gs} of M1 for a long time, which is similar to the S/H circuit in [2]. Concurrently with the retention, a potential difference between a gate of M3 and a source of M1 is also retained, so that a variation in V_{ds} of M1 is suppressed. Thus, M3 functions as a cascode device. With this configuration, a cascode amplifier with a high amplification factor is obtained.

The input-signal voltage is at the GND level as shown in Figure 2. The IGZO-FETs that are NMOS have a difficulty in having a reaction to signals at the GND level. In contrast, high voltages are applied to a back gate of an input FET to shift the threshold voltage negatively, and the voltage between the back gate and the source is retained by the S/H circuit, so that signals at the GND level is detected.

4. Experimental Results of the CMC

With use of 0.36 μm IGZO-FET technology, a CMC was fabricated using approx. 12,000 transistors (W/L = 0.36 μm/0.36 μm). The chip area is 680 μm × 2000 μm (Figure 5). Figure 6 shows output frequencies with respect to input voltages. The output frequencies monotonically increase as the input voltage value increases. The linearity is broken along

with an increase in the input voltage. However, data compensation is possible in a digital circuit with use of compensation data prepared in advance.

5. Conclusions

A CMC using only IGZO-FETs, where a cascode amplifier achieves a high amplification factor with use of an S/H circuit with low leakage current, has been fabricated. With such a configuration, signals at the GND level is detected by control of a back gate of an input FET.

References

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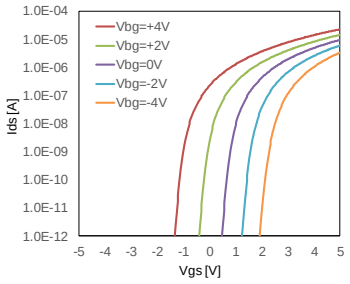

Fig. 1 Off-state current and back-gate voltage dependence of thresh-old voltage.

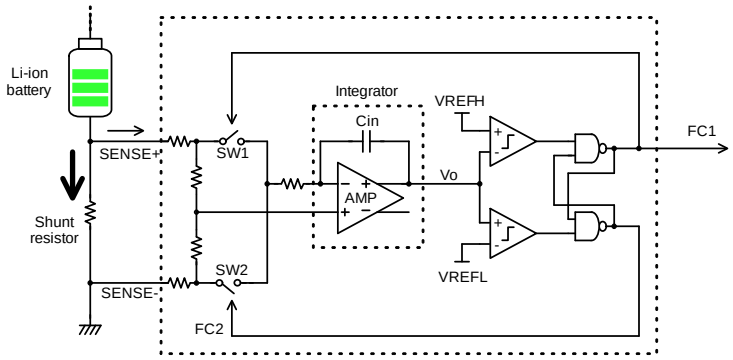

Fig. 2 CMC (V-F converter)

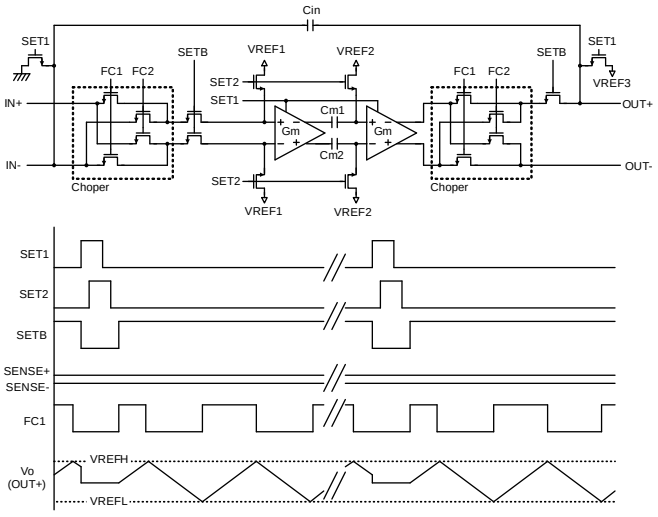

Fig. 3 Amplifier of Integrator and operation timig diagram

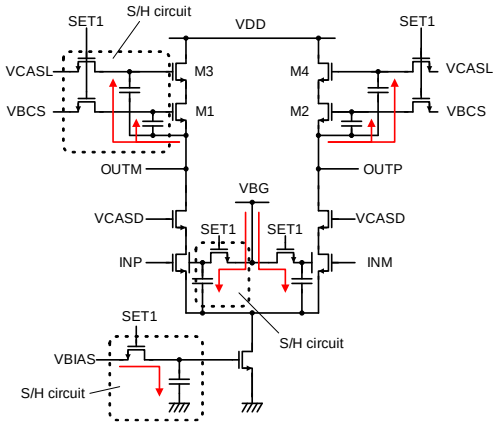

Fig. 4 Transconductance Amplifier Gm (Cascode Amplifier)

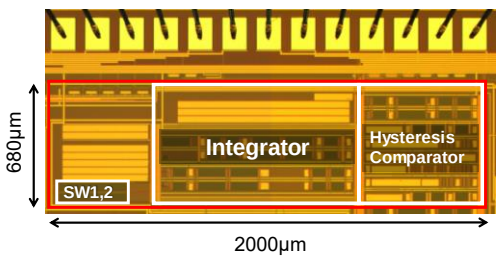

Fig. 5 Chip die

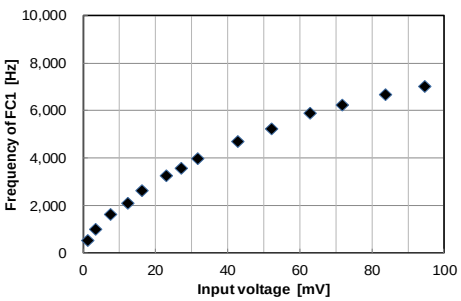

Fig. 6 Input voltage v.s. output frequency of CMC.