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Integrated Simulation Methodology for EM-induced Circuit Degradation

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Abstract

An integrated methodology to simulate circuit degradation due to electromigration (EM) is proposed. Based on a proposed dynamic resistance evolution model including layout effects, the methodology enables SPICE to perform circuit EM reliability simulation with circuit simulation concurrently, without additional aging simulation steps. Simulation results show accurate predictions of the circuit degradation behavior due to EM.

1. Introduction

Interconnect reliability is a major concern with the continuous scaling of technology due to electromigration (EM) [1]. In most cases, EM causes a gradual time-dependent resistance change, instead of an abrupt failure in the interconnect wires. To accurately predict the dynamic circuit degradation behavior due to EM, a methodology that able to capture the incremental changes of resistance and circuit performance is needed. Traditional methods rely on SPICE based circuit simulation to obtain the waveform in individual node and then use the Black's equation in a standalone program taking the node voltages as to obtain the EM degradation parameters, such as mean time to failure and failure rate. The obtained parameters are then used to determine if circuit design meets the reliability requirement. In this work, an integrated simulation methodology is proposed to analyze EM reliability from circuit performance together with the SPICE simulation without the need for post-simulation treatment.

2. Integrated Simulation Methodology

The proposed method assumes that the post-layout extraction is performed to construct the netlist consisted of resistors representing the interconnect wire resistance. The subsequent interconnect simulation process is shown in Fig.1. The initial geometry parameters such as length, width and resistance value can be obtained from the layout extractor or directly input by users. Users combine the layout parameters of all interconnect, EM parameters with circuit simulation parameters to form as an input file of SPICE simulator. Then the spice simulator executes the circuit and degradation simulation concurrently. After each simulation time step, the output file from SPICE records the change of interconnect resistance, characteristics of circuit and EM degradation results at every time point until the required simulation time. Finally, users can determine the designed circuit whether satisfy their reliability requirement based on the simulation results.

3. Dynamic EM Model

To realize the proposed methodology, a dynamic resistance evolution model of interconnect metal line is developed as [2]:

$$R(t+\Delta t) = R_0 + \frac{\rho_{Cu} L_{crit}}{A_{Cu}} \left(\frac{L_{crit}}{v_e (t_{eq} + \Delta t)} - 1 \right)^{-1}. \quad (1)$$

$$where \quad v_e = \frac{D}{kT} Z^* e \, \rho_{Cu} J_{eff}.$$

Where R_0 is the initial resistance before void formation. A_{cu} and ρ_{Cu} are cross area and resistivity of the copper line (1.68×10^{-8} Ωm). L_{crit} represents the critical void length. The void growth rate v_e, also defined as the void edge drift velocity [2]. Z^* is the effective nuclear charge with value of 1. D is effective diffusion constants (6.5×10^{-5} m^2/s). The effective current density J_{eff} is defined as (J - J_{crit}). The critical current density J_{crit} is derived from the short lead effect. A time variable t_{eq} is used to capture the dynamic nature of resistance change. Δt is the time step for a given stress current and t_{eq} is the equivalent stressing time under the present stressing current as accumulated from the beginning of the process. With this method, a resistance change over a small time interval can be obtained.

$$t_{eq} = \left[\frac{\left(R_{(t)} - R_0 \right) \times A_{Cu}}{L_{\mathrm{crit}} \rho_{Cu}} + 1 \right] \times \frac{L_{\mathrm{crit}}}{v_e}. \quad (2)$$

To capture the circuit level EM dependence on interconnect structure, the effective critical current density under the effect of reservior and sink are also included as $J_{crit,R}$ and $J_{crit,S}$, respectively[3]:

$$J_{crit,R} = \left(\frac{L + L_R}{L} \right) J_{crit}, \quad J_{crit,S} = \left(\frac{L + L_S}{L + 2L_S} \right) J_{crit}. \quad (3)$$

4. Circuit Simulations

Fig. 2 shows the resistance change of one metal line between simulation results of our methodology and experimental data [4]. For both DC stress and pulse signal, the developed method shows accurate prediction of the resistance change due to EM. The H-clock tree is also simulated with the schematic structure shown in Fig. 3. After simulation, the failed buffer line structure is pointed out in Fig.3. The changes of resistance of the corresponding failed interconnect segments are shown in Fig. 4, which directly show the change of interconnect segments with time and different change rates with interconnect segments. These results indicate layout dependent effects cause different change rate of metal lines of

circuit. The output signal degradation of buffer line after different EM degradation simulation time is shown in Fig. 5. The slew rate of the output signal degrades with time, providing circuit designers with a direct quantitative indication of the signal delay due to EM. Fig. 6 shows the effect of different widths on the delay time performance degradation. The EM induced degradation in signal delay becomes worse with a smaller interconnect size. Especially below 100nm, EM degrades the circuit performance so much that the H-tree clock tree will cause significant delay time after 3 years. These simulation results show that the proposed integrated simulation methodology accurately predicts not only the dynamic resistance change versus time, but also the degradation of circuit performance due to EM, which gives another perspective to check if circuit design meet the reliability requirements.

5. Conclusions

An integrated simulation methodology that can accurately simulate circuit degradation due to EM is proposed. It reduces the simulation complexity with one SPICE run.

Acknowledgements

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References

[1] M. Meyer *et al*, Microelectronic. Engineering, **64** (2002) 375.
[2] M. Hauschildt *et al*, J. Appl. Phys. **101** (2007) 4.
[3] M. Lin and A. Oates, IEEE TDML. **13** (2013) 322.
[4] K.-D. Lee, *IEEE IRPS*, 2012.

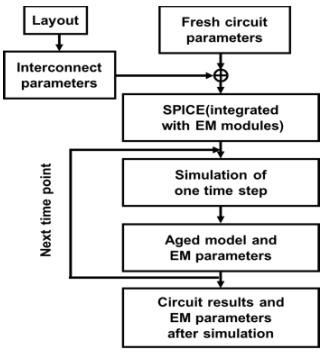

Fig. 1 The flow chart of proposed EM simulation methodology.

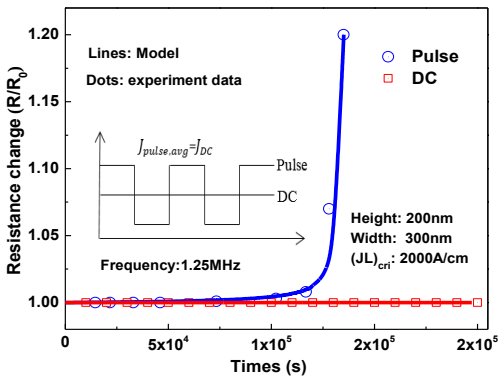

Fig. 2 Comparison between simulation with the proposed method and experiment data of metal line [4].

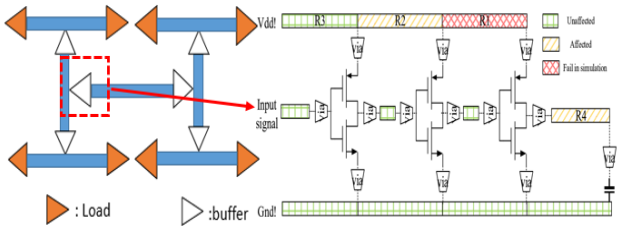

Fig. 3 The schematic of H clock tree circuit in simulation and failed buffer line structure after simulation. (height and width of metal line are 200nm and 140nm, 1GHz Frequency, $(JL)_{cri}$ is 3500A/cm).

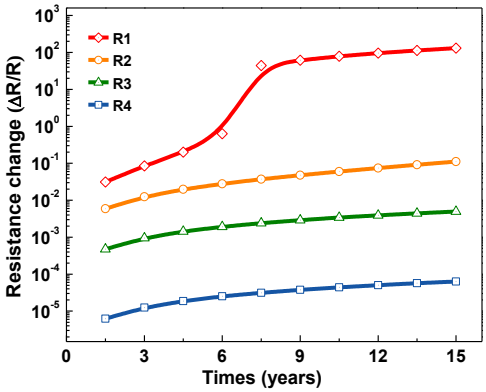

Fig. 4 The resistance change of different interconnect segments of failed buffer line in circuit EM degradation simulation.

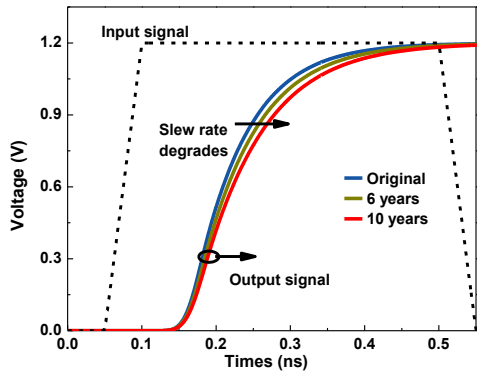

Fig. 5 Output signal of corresponding buffer line after EM degradation simulation under 1GHz frequency.

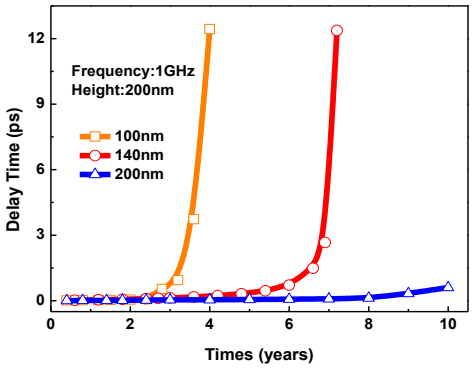

Fig. 6 Delay time of corresponding buffer line simulation with different width of interconnect wire.