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Chip-to-Wafer Gang Bonding for High Throughput 3D-Integration

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Abstract

A chip-to-wafer (c2w) stacking process has been developed and tested on 8" and 12" wafer using the test vehicle chip containing 10 µm x10 µm CuSn µ-bumps. c2w stacking process was optimized for thickness of the underfill-laminate, pre- and post-bonding temperature and pressure. It is found that with only pre-bonding, the c2w process yield is very low. The yield for c2w bonding process is highly enhanced by the post-bonding. While for relatively thicker underfill-laminate, the alignment accuracy has been improved by reducing the post-bonding pressure.

Keywords: chip-to-wafer, µ-bump, Cu-Sn, NCF

1. Introduction

3D-integration is now inalienable technology in semiconductor industry worldwide to realize the high performance edge devices. Although 3D-LSI/IC can be realized in several ways as shown in table 1, the chip-to-wafer (c2w) bonding technology [1-4] has been gaining momentum because of its performance improvement and cost effectiveness. Although wafer-to-wafer (w2w) level integration is favorable in terms of throughput, but the yield goes down dramatically when increase the number of tiers. On the other, the yield is tremendously high in the chip-to-chip (c2c) integration process (since only known-good-dies, KGD are used), but the throughput is extremely low. Whereas in the c2w the yield is high (only KGDs are used) and throughput is also better than c2c, since the BEOL processes such as TSV formation, µ-bumping, etc. are done at wafer level.

Though c2w seems to be promising than the c2c or w2w level processes, the bonding process in c2w is somewhat complicated as compared to the bonding in c2c or w2w processes. As shown in fig. 2, the substrate temperature cannot be kept at the bonding temperature, and it is because, 1) the surface of the landing pad or the µ-bumps gets deteriorated in the yet to be bonded region, and 2) the already bonded chips are subjected to thermal hysteresis, and it is proportional to the number of chips. Thus one need to find optimum pre-bonding parameters. This problem is further aggravated if the chips are pre-laminated by nonconductive film (NCF) underfill.

In the present study, we report the experimental results on c2w bonding for 8"/12" substrate test vehicle with CuSn µ-bump laminated with NCF underfill.

2. Experimental

A test vehicle containing 10 µm x 10 µm CuSn µ-bumps on both the bottom substrate and top chip wafers were formed by conventional BEOL process. After the bumping process, top chip wafer was diced into chips after the NCF was laminated. The dimensions of the top chips and bottom package area are shown in table 2. c2w bonding was carried out in two step process; diced KGDs were first pre-bonded at lower substrate temperature (room temperature) using flip-chip bonder. Then the pre-bonded chips were gang bonded at higher temperature (at 250 °C for 1 min in vacuum). c2w bonded samples were tested for electrical and morphological features by I-V and SEM observation.

Table 1. Comparison of 3D Stacking Methods

Stacking method	Chip-to-Chip	Wafer-to-Wafer	Chip-to-Wafer	Advanced Multichip-to-Wafer
Throughput	Extremely Low (one by one)	High (batch processing)	Low to medium (pick & place)	High (self-assembly)
Yield	High (use of KGD)	Low	High (use of KGD)	High (use of KGD)

3. Results and Discussion

Shown in fig.2 and 3 are cross-sectional (x-sec.) SEM images for top chip µ-bump before and after reflow, respectively. In our study it was found that if the solder was not reflowed before bonding, it leads to the NCF trapping inside the µ-joint formed after post-bonding. It is generally expected that the reflowed µ-bumps helps to repel the NCF, since the surface is not corrugated unlike the surface of pristine µ-bumps.

Fig. 4 depicts the x-sec. SEM images for c2w sample, before and after gang bonding. The initial NCF thickness on the top chip was around 13 µm, and it has been reduced to ~11 µm after post-bonding. We have varied the NCF thickness from 7 µm to 18 µm. We found that NCF is left inside the µ-joint in the pre-bonding only sample. Whereas after post gang bonding, we did not observe any presence of NCF inside the µ-joint. Fig. 6 depicts the SEM images of typical gang bonded c2w sample with no NCF left inside the µ-joint, with an alignment accuracy of ~1 µm. It is that for relatively larger bonding pressure, we have obtained better electrical and mechanical characteristics, which is owing to the complete removal of underfill laminate in between the top and bottom µ-bumps after c2w bonding.

Shown in fig. 5 is the optical microscopic images obtained for c2w gang bonded chips (NCF pre-laminated) on 8" LSI substrate. Since the c2w integration was carried out for only 16 % of the substrate bonding area, the landing pads (µ-bump) in the bottom substrate are visible. The gang bonded top chips are shown by arrows.

In summary, upon optimizing both pre- and post-bonding parameters, we have been able to successfully carryout c2w integration on 8" LSI substrate using NCF pre-laminated chips. Microstructural (SEM) analysis revealed that there is no NCF material left behind inside the µ-joint area, and it also is free of voids at the µ-bump space region.

References: [1] P. Ramm *et al*, SSDM 2003; [2]T. Fukushima *et al,* ECTC 2007; [3]T. Fukushima *et al*.IEEE TED2012; [4]N. Asahi *et al*,ICEP 2018.

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Table 2. Test Vehicle Dimensions

Top die	
Die size & thickness	5 mm x 5 mm & 50 ~ 750 μm
Bump height	Cu 4 μm; Ni 2 μm & Sn 4 μm
Bump size & pitch	10 μm x 10 μm & 20 μm
NCF thickness	13 μm
Bottom Substrate	
Package size & thickness	8 mm x 8 mm & 750 μm
Bump height	Cu 4 μm; Ni 2 μm & Sn 4 μm
Bump size & pitch	10 μm x 10 μm & 20 μm

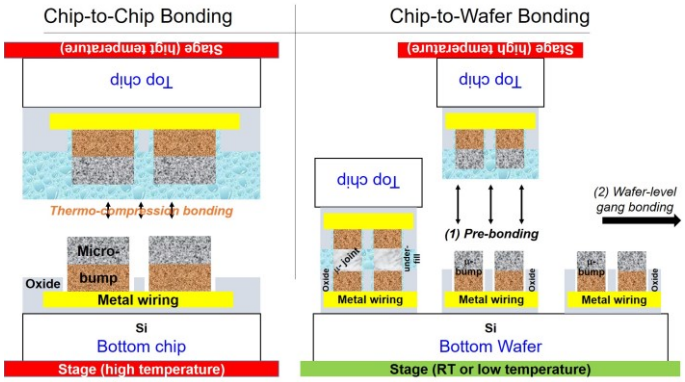


Figure 1. Schematic illustration of c2c and c2w stacking process for 3D-LSI fabrication.

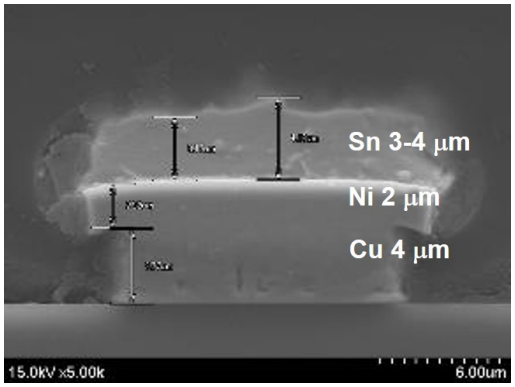


Figure 2. X-sec. SEM image revealing the components present in the 10 mm x 10 mm size Cu-Sn pristine μ-bumps, before the reflow process.

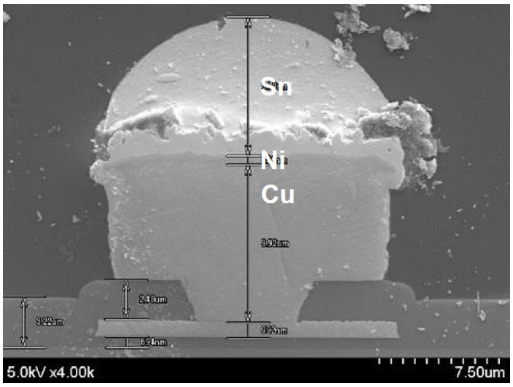
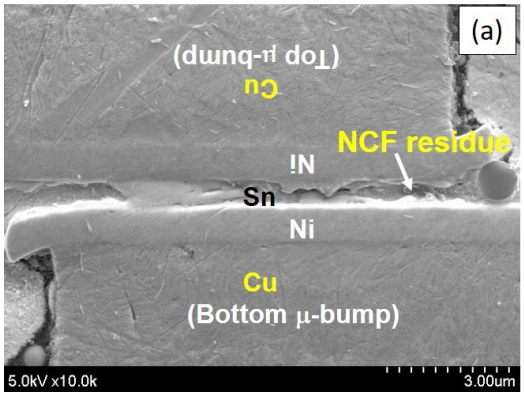


Figure 3. X-sec. SEM image revealing the components present in the 10 mm x 10 mm size Cu-Sn pristine μ-bumps, after the reflow process.



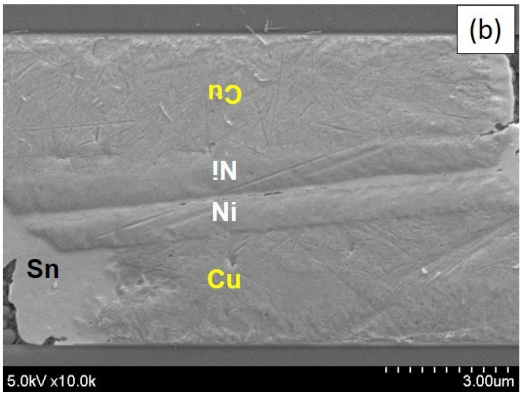


Figure 4. X-sec. SEM images (a) after pre-bonding and (b) after post gang bonding revealing the necessity of post bonding in c2w stacking process.

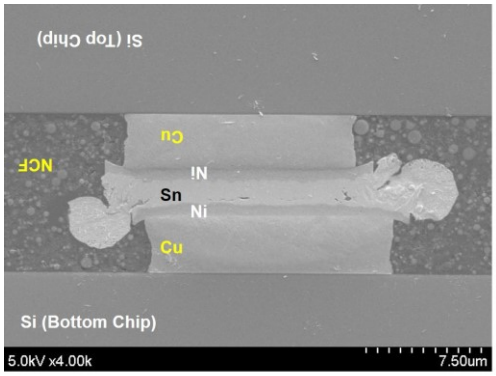


Figure 5. X-sec. SEM images revealing the successful μ–joint formation after c2w post gang bonding process on 8" LSI wafer.

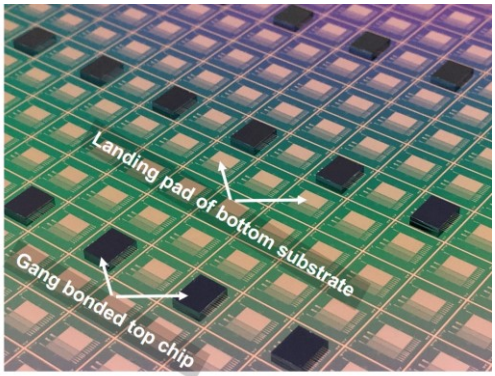


Figure 6. Optical microscopic image taken after the c2w stacking process on 8" LSI wafer.