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Evaluation of Carrier Recombination Lifetime in Silicon Epitaxial Layer by Open Circuit Voltage Decay Method

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Abstract

A new technique of evaluation for the carrier recombination lifetime in silicon epitaxial layer was invented based on the principle of Open Circuit Voltage Decay. PIN diodes that have different junction areas were fabricated on silicon epitaxial wafer and true recombination lifetime in epitaxial layer and surface recombination velocity on sidewall of mesa structure were evaluated.

1. Introduction

The carrier recombination lifetime is an effective parameter to characterize the purity of semiconductor materials and devices. Microwave-Photoconductive Decay (μ-PCD) method is often employed to evaluate difference in recombination lifetime in a wafer or between wafers, by creating two dimensional lifetime map. [1][2]. However the μ-PCD has a difficulty to measure the recombination lifetime of silicon epitaxial layer which adopts the highly-doped substrate. The sheet conductance of epitaxial layer after carrier injection is relatively small as compared to that of highly-doped substrate. Therefore the total decay of sheet conductance from the epitaxial wafer mostly does not change [3]. Differential μ-PCD was also proposed to evaluate the recombination lifetime of thin films [4]. However this method can not completely exclude effect of surface recombination. The Open Circuit Voltage Decay (OCVD) method measures recombination lifetime in the base region in PIN diodes. Accordingly, the carrier recombination lifetime of epitaxial layer can be evaluated by employing the epitaxial layer as the base region of PIN diode [5]. However this method typically uses discrete PIN diode structure. Thus, the structure can never remove the effect of surface recombination on the side wall of PIN diodes. To resolve these problems and difficulties in the conventional techniques, here we try to evaluate true recombination lifetime of the silicon epitaxial layer by taking advantage of the OCVD method.

2. PIN diode structure & Measurement

Two silicon epitaxial wafers that have high and low recombination lifetime (Wafer A and Wafer B) were prepared. These wafers are phosphorus-doped 200mm n/n+ silicon epitaxial wafer. Resistivity and thickness are 17.5Ωcm and 40μm for epitaxial layer, and 0.0015 Ωcm and 77.5μm for substrate, respectively. Figure.1 shows schematic cross section of the epitaxial layer structure. To fabricate PIN diodes on the silicon wafers, p+ epitaxial layer was grown by Chemical Vapor Deposition (CVD) process, on these epitaxial wafers. Resistivity and thickness of p+ layer are 0.1Ωcm and 2μm.

PIN diode mesa structures were fabricated by photolithography and chemical dry etching. Figure.2 (a) shows schematic illustration of patterning on the silicon wafers. Totally, 138 cells were regularly patterned on the epitaxial wafers. Figure.2 (b) shows PIN diodes within a unit cell. One unit cell possesses 4 PIN diodes that have different junction areas: 0.01, 0.04, 0.10, and 0.81 cm^2. These diodes within a unit cell were employed to remove surface recombination effect on side wall of the mesa structures, which refers at later section.

The OCVD measurement system was connected with manual prober and wafer center (pink filled color area in Fig.2(a)) was measured to compare recombination lifetime between Wafer A and B.

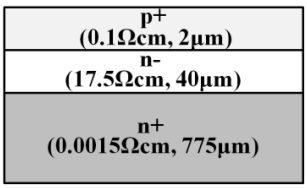

Figure.1 Schematic illustration of the epitaxial layer structure for the OCVD measurement.

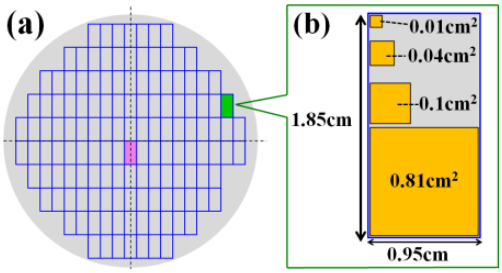

Figure.2 Schematic illustrations of (a) pattern on the silicon epitaxial wafers and (b) mesa structures within a unit cell.

3. Results

In the OCVD measurement, recombination lifetime in high level injection condition (τ_{hl}) and low level injection condition (τ_{ll}) can be calculated by following equations:.

$$\tau_{hl} = -\frac{2kT/q}{dV/dt}. \quad (1)$$

$$\tau_{ll} = -\frac{kT/q}{dV/dt}. \quad (2)$$

where, k, T, q, V, and t are Boltzmann constant, temperature, elementary charge, measurement voltage, and time. Figure.3 shows measurement results of voltage decay curves in each diode of Wafer B. Inflection point of voltage decay curves was recognized at 0.4V (red dashed line). Therefore, τ_{hl} and τ_{ll} were estimated from 0.5-0.4V and 0.4-0.3V, by employing slopes of linear approximation lines that are equivalent to the dV/dt. To compare recombination lifetimes of the epitaxial layer in Wafer A and B, the surface recombination effect should be removed. In this experiment, bare silicon which acts as strong surface carrier recombination center exposes on the side wall of mesa structures. True recombination lifetime of the epitaxial layer in high ($\tau_{bulk,hl}$) and low level injection condition ($\tau_{bulk,ll}$) can be calculated from below equations :

$$\frac{1}{\tau_{hl}} = \frac{1}{\tau_{bulk,hl}} + \frac{Sv_sD_a}{V(D_a - Lv_s)}. \quad (3)$$

$$\frac{1}{\tau_{ll}} = \frac{1}{\tau_{bulk,ll}} + \frac{Sv_sD_p}{V(D_p - Lv_s)} \quad (4)$$

where S, V, v_s, D_p, D_a, and L are area of side wall, volume of mesa structure, surface recombination velocity, diffusion coefficient of hole, ambipolar diffusion coefficient, and carrier diffusion length. The true recombination lifetime of epitaxial layer and the surface recombination velocity were obtained from interception and slope of approximation line which is drawn by plotting reciprocal values of lifetime and ratio of S and V, in each mesa structure. Figure. 4 shows $1/\tau_{hl}$ and $1/\tau_{ll}$ vs S/V plots (filled circles) and linear approximation lines (dot lines).

The calculation results were summarized in Table I. The true recombination lifetime values of Wafer A are higher than the value of Wafer B. This relationship of the true recombination lifetime values is consistent with before fabrication of PIN diodes for the OCVD. The surface recombination velocity in low level injection is higher than the values in high level injection, in each wafer. This implies carrier injection level dependence of surface recombination velocity [6].

4. Conclusion

Evaluation of the carrier recombination lifetime in silicon epitaxial layer was carried out by employing the OCVD method. Unit cells that possess different junction areas of PIN diode mesa structures were regularly fabricated on the silicon epitaxial wafers and were employed to evaluate the true recombination lifetime values in the epitaxial layer, by removing the effect of surface recombination on the side wall of mesa structures. Relationship of the true recombination lifetime values between two wafers showed consistency with before mesa fabrication. As to the surface recombination velocity, dependence of carrier injection level was confirmed.

5. Reference

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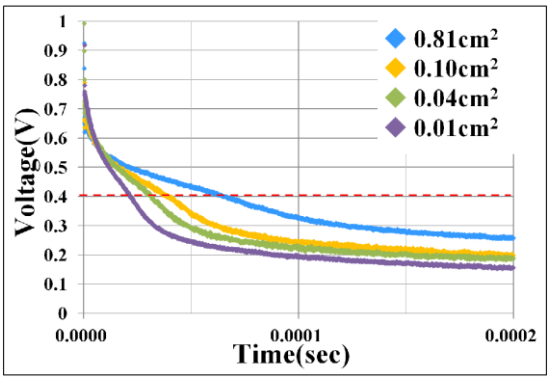

Figure.3 The OCVD measurement results of PIN diodes, within the unit cell of Wafer B.

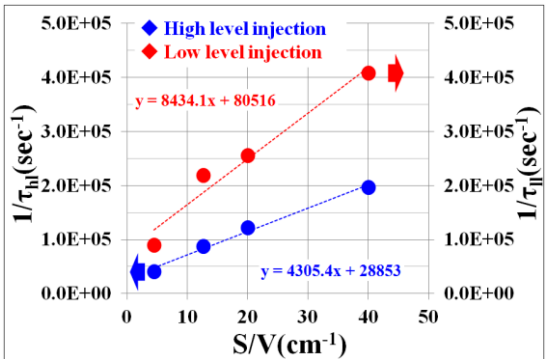

Figure.4 $1/\tau_{hl}$ and $1/\tau_{ll}$ vs S/V plots (filled circles) and approximation lines (dot lines) of Wafer A.

Table I Calculation results of $\tau_{bulk,hl}$, $\tau_{bulk,ll}$, and v_s.

Wafer	$\tau_{bulk,hl}$ (µsec)	$\tau_{bulk,ll}$ (µsec)	v_s (cm/sec)	
			High level	Low level
Wafer A	49.27	24.14	535.8	665.6
Wafer B	34.65	12.42	610.0	880.4