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Study on the Effects of Si Implantation on the Interface of 4H-SiC MOSFET

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Abstract

In this study, Si implantation was used to improve the interface properties of SiC/oxide in 4H-SiC MOSFETs. In lateral MOSFETs, 4-6% improvement on the linear and saturation was observed with Si implantation. From high-low frequency C-V measurements, Si implanted MOS-capacitor shows 20% lower interface state density than non-implanted one at an energy level of E_C-E = 0.2 eV, without degrading oxide integrity. Increase of 7.6 times saturation current enhancement by Si implantation in vertical DMOSFETs was observed.

1. Introduction

4H-SiC is an attractive material for power devices because of the wide bandgap, high critical electric field, good thermal conductivity etc. However, field effect devices in SiC face high channel resistance owing to low inversion layer mobility and high interface state density. Previous study reports germanium (Ge) implanted Si NMOSFETs gains field effect mobility improvement with a lower threshold voltage of MOSFET [1]. In this study, another species of group 4 elements, Si, was introduced through implantation to modify the interface properties of 4H-SiC MOSFETs.

2. Experiment

Lateral MOSFETs were made on a 4H-SiC N^- epilayer with a doping concentration 8×10^{15} cm^{-3}. After wafer clean, the p-well, S/D and body region were formed by high temperature implantation using species of Al, P, and Al respectively. After dopant activation at a high temperature, Si implantations on three wafers with total dose of 1×10^{14} cm^{-2}, 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2} were done at a temperature of 500°C. A baseline wafer without Si implantation was also processed in parallel to compare with Si implant splits described above. The gate dielectric was thermally grown and annealed in an N_2O ambient to passivate the traps. The gate dielectric thickness formed was about 47 nm from the measured Cox for all the wafers. The gate electrode was N type polysilicon and S/D contacts were formed by Ni silicide.

3. Measurement results and discussion

DC Characteristics of Lateral MOSFETs

The measured lateral MOSFET is an n-type MOSFET with a channel width and a length of both 100 μm. Fig. 1 shows the MOSFET transfer characteristics when the Vds bias is at 0.1 V. It can be observed that the threshold voltages of four wafer splits are nearly the same, about 5 V defined at Ids = 0.1 μA. However, the best Si implanted MOSFETs have larger Idlin, about 6% increase compared with the baseline, at Vg=20V. Fig. 2 shows the increase in Idsat of Si implanted wafers, about 4% larger than baseline, at Vgs = 20 V and Vds = 20 V.

Dielectric Properties

The interface state density (D_{IT}), which was deduced by high-low frequency capacitance measurement on NMOS-capacitors, is shown in Fig. 3. Si implanted samples show smaller D_{IT}, about 20%, than non-implanted baseline one at an energy level of Ec-E = 0.2 eV, which should benefit the conduction of an n-channel MOSFET. However, Si implanted NMOS-caps have a larger D_{IT} deep in the energy band, which is very slow responding and less critical for practical applications. Fig. 4 shows the dielectric breakdown measurement results. The leakage and breakdown behaviors of these wafers with and without Si implant are nearly identical.

Minority Carrier Lifetime

In previous studies it was shown that minority lifetime in SiC can be enhanced by carbon implantation [2], because carbon atoms diffuse and eliminate a critical lifetime killer defect, carbon vacancy. As a result, the conductivity modulation and the forward voltage (V_F) of a PIN diode in SiC is significantly improved. Here we summarize the forward characteristics of the body diodes inherent in the lateral MOSFETs in Fig. 5. V_F increases with the dose of Si implantation which implies the decrease of minority carrier lifetime in SiC. This phenomenon can be explained as the opposite effect of carbon implantation and is a direct evidence that implanted Si atoms diffuse in the crystal and modify the properties at the interface as well as the bulk.

DC Characteristics of Si implanted DMOSFETs

Si implantation was also employed on SiC DMOSFETs. Fig. 6 shows the measured results. Compared to the baseline DMOSFET without Si implantation, the saturation current (Idsat) of Si implanted DMOSFET, at Vgs = 5 V, is increased by 7.6 times. The Ron,sp is reduced from 5.6 to 4.0 $m\Omega cm^2$. This enhancement may also come from other parts of the device structure affected by Si implantation such as contact resistances other than the channel. Further investigation is under way.

4. Conclusions

Si implantation on lateral 4H-SiC MOSFETs shows about 5% improvement in the forward characteristics. The saturation current of vertical DMOSFETs was also improved. Si implantation shows no degradation on the oxide leakage and breakdown characteristics.

Acknowledgements

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References

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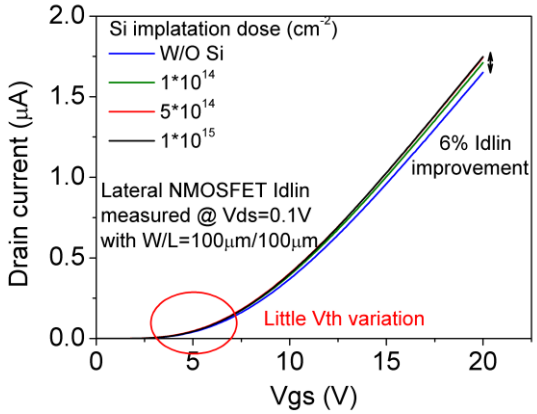

Fig. 1. Transfer characteristics of Si implanted lateral SiC MOSFETs. Idlin is increased by 6% by Si implantation.

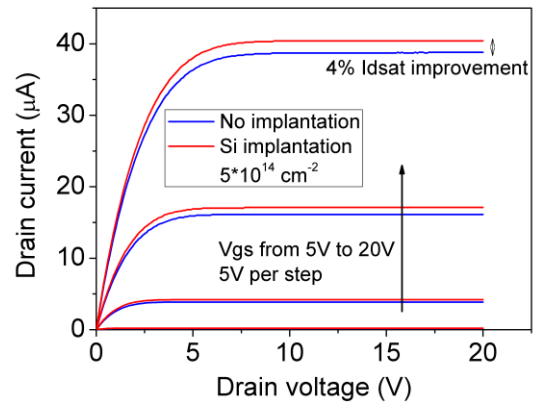

Fig. 2. Id-Vd curves of Si implanted SiC MOSFETs. Idsat is increased by 4% by Si implantation.

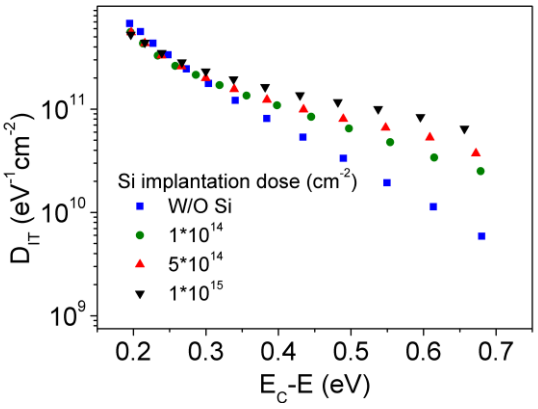

Fig. 3. D_{IT} of Si implanted NMOS-capacitance. 20% reduction in D_{IT} near conduction band is observed.

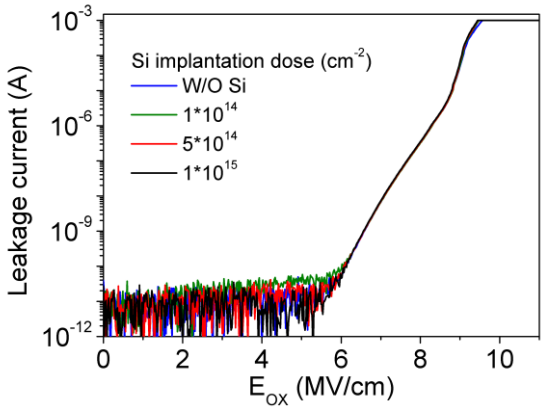

Fig. 4. Leakage current and breakdown characteristics of Si implanted Si MOS capacitors.

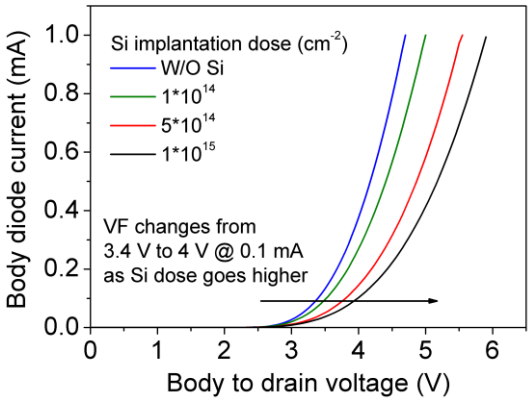

Fig. 5. Forward characteristics of the body diode in the Si implanted lateral MOSFETs.

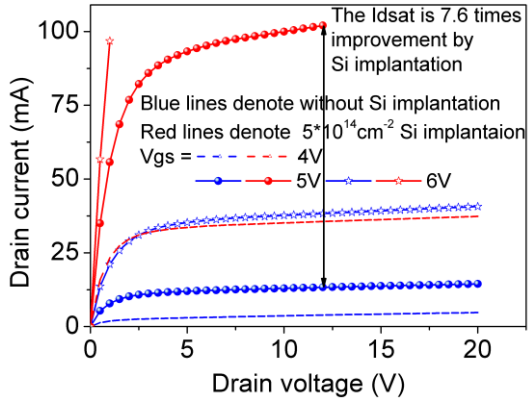

Fig. 6. Id-Vds of Si implanted DMOSFET compared with non-Si implanted baseline. Increase in saturation current is observed. The Idsat of Si implanted DMOSFET at Vgs=5V is 7.6 times larger than that of the baseline one.