Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp753-754

Effects of Deep Level States Generated by Mg-Ion Implantation on Electrical Properties of GaN MOS Diodes before Activation Annealing

Ryo Kamoshida, Shunta Murai and Masamichi Akazawa

Hokkaido University
Kita 13, Nishi 8, Kita-ku, Sapporo 060-0813, Japan
Phone: +81-11-706-6875 E-mail: akazawa@rciqe.hokudai.ac.jp

Abstract

The effects of deep level states on electrical properties of MOS diodes with moderately Mg-ion implanted GaN before activation annealing were studied. A sign of surface Fermi level pinning was indicated in the capacitance–voltage and capacitance–frequency (*C–f*) characteristics of the fabricated MOS diode. The interface state density D_{it} distribution extracted from the *C–f* characteristics showed a discrete level between 0.2 and 0.3 eV below the conduction band edge. Simulation results indicated that a bulk deep level at the same energy position can cause Fermi level pinning at the surface. Considering that the D_{it} distribution should be usually U-shaped, the extracted discrete level is highly likely the bulk deep level in Mg-ion implanted GaN. The origin of the deep level is also discussed.

1. Introduction

GaN is a promising wide-gap material for power electronic devices because of its high saturation electron velocity, high break down field, and good thermal conductivity. In the fabrication of electronic devices, the ion-implantation is a very useful technique for selective doping. However, formation of a p-type region by this technique has been difficult. Recently, successful doping by Mg-ion implantation has been reported [1 – 3]. Nevertheless, the effects of deep levels generated by Mg-ion implantation on electrical properties of GaN have not been clarified completely. To clarify this issue, electrical measurement should be carried out carefully before activation annealing at a high temperature (> 1,200 ºC).

In this presentation, it is reported that a deep level causes anomalous electrical properties of MOS diodes with moderately Mg-ion implanted GaN before activation annealing, and the dominant deep level is extracted from the anomalous properties.

2. Experimental

An n-type (n = 5×10^{17} cm^{-3}) GaN epitaxial layer was grown on a conductive c-plane free-standing GaN substrate by MOCVD. Mg-ion implantation was carried out at room temperature with an energy of 50 keV, an angle of 7º, and a dosage of 1.5×10^{12} cm^{-2}. After, ion implantation, a 30 nm thick Al_2O_3 layer was deposited by atomic layer deposition (ALD) using trimethylaluminum and H_2O at 300 ºC. Ni/Au top electrodes and a Ti/Au back ohmic contact were formed by electron beam evaporation to complete a MOS structure. Finally, post-metallization annealing for reducing the interface state density was carried out at 300 ºC in air. For completed MOS diodes, capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) measurements were carried out. A numerical simulation of band bending was done by using a previously developed computer program [4].

3. Results and Discussion

The *C–V* curves measured in a high frequency range for the completed MOS diode are shown in Fig. 1. It can be seen that a wide plateau exists under the minus bias and that the oxide capacitance C_{OX} is not achieved even at a high plus bias of 10 V. The total capacitance change under the plus bias becomes smaller as the measurement frequency increases, which indicates that the high frequency limit approaches asymptotically to a flat characteristic. This tendency indicates severe Fermi level pinning at the GaN surface.

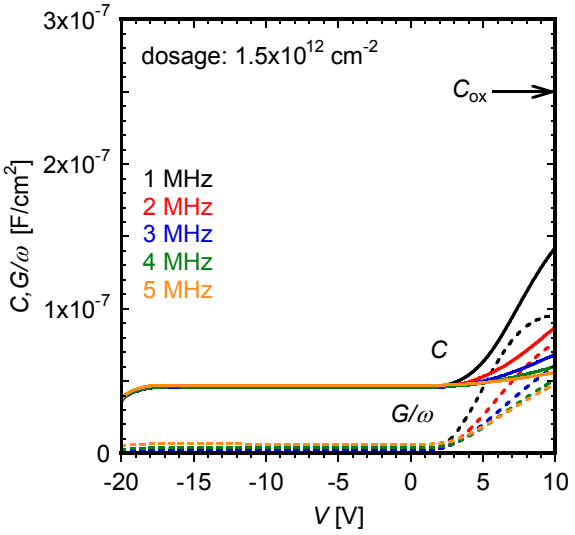

Fig. 1 *C–V* curves measured for the completed MOS diode at a high frequency range.

The sign of surface Fermi level pinning was also indicated by the *C–f* characteristics measured for the same MOS diode as shown in Fig. 2. It can be seen that the *C–f* curves shift to higher frequency as the bias voltage increases. It should be noted that the capacitance converges to the same value of 5×10^{-8} F/cm^2 independent of the bias voltage as the frequency increases. In addition, the horizontal shift converges with the bias voltage. This indicates an abrupt increase of the interface state density D_{it} exists in the band gap to pin the Fermi level.

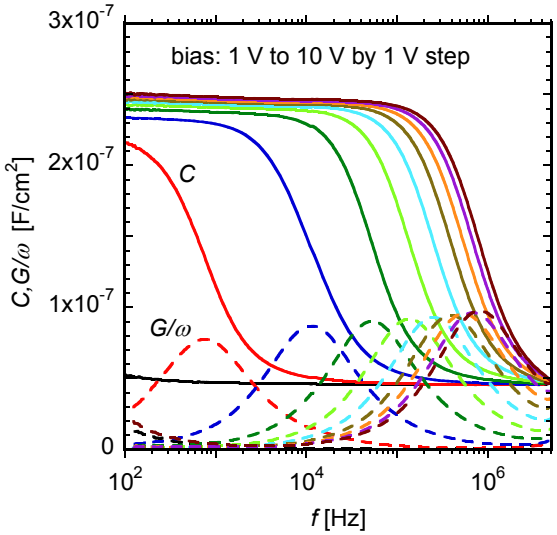

Fig. 2 *C*–*f* curves measured for the completed MOS diode.

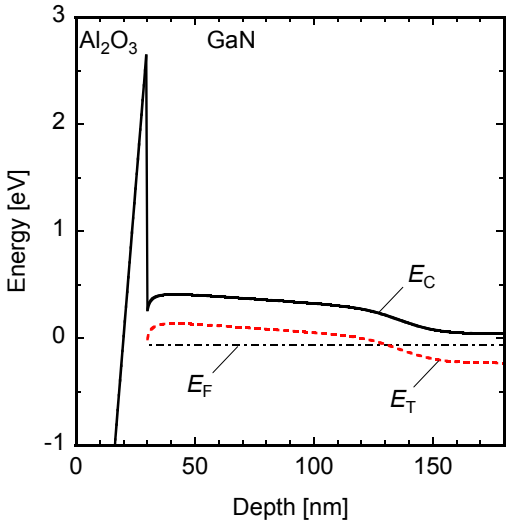

Fig. 4 Simulated band bending at bias voltage of 9 V.

The D_{it} distribution extracted from the *C*–*f* characteristics by using the conductance method is plotted in Fig. 3. Here, the capture cross section was assumed to be 1×10^{-16} cm^2. A discrete state can be seen. However, according to the disorder-induced gap state model [5], interface states are originated from interface disorder and the D_{it} distribution should be U-shaped. Therefore, there is possibility that the extracted discrete state is originated from a bulk defect.

An example simulation result for band bending assuming a discrete bulk deep level E_T at $E_C - 0.27$ eV is shown in Fig. 4. The density profile on this level was assumed to be exponential decay from the GaN surface referring to the TRIM simulation results for vacancy defects. We found that the bulk deep level pins the Fermi level E_F at the surface, while the capacitance is determined by the deeper cross point of E_F and E_T. This result supports the assignment of the extracted discrete level to the bulk deep level. According to the previous report [6], the origin of this deep level is possibly a divacancy V_{Ga}–V_N. This result is in good agreement with the results of positron annihilation spectroscopy [7].

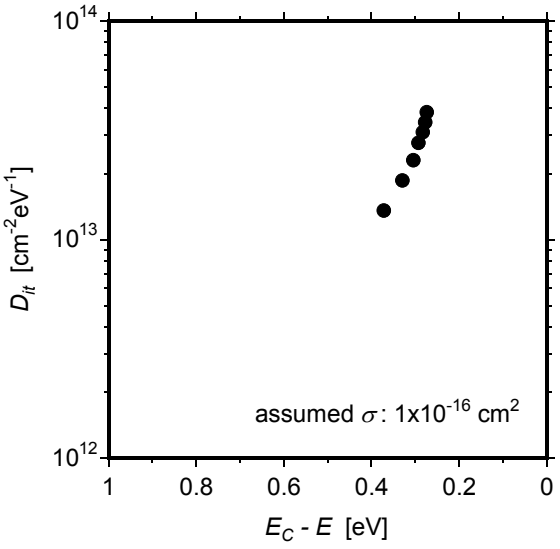

Fig. 3 D_{it} distribution extracted by conductance method.

4. Conclusions

The electrical properties of MOS diodes with moderately Mg-ion implanted (dosage: 1.5×10^{12} cm^{-2}) GaN before activation annealing have been investigated. Anomalous *C*–*V* and *C*–*f* characteristics were found to be resulted from a bulk deep level at 0.2 – 0.3 eV below E_C generated by Mg-ion implantation. The origin of this deep level is possibly V_{Ga}–V_N.

Acknowledgements

The authors appreciate Dr. T. Narita of Toyota Central R&D Labs., Inc. for providing the GaN epitaxial wafers. This research is supported by the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan, through its "Program for research and development of next-generation semiconductor to realize energy-saving society."

References

[1] J. D. Greenlee, T. J. Anderson, B. N. Feigelson, K. D. Hobart and F. J. Kub, Phys. Status Solidi A **212**, 2772 (2015).

[2] T. Oikawa, Y. Saijo, S. Kato, T. Mishima and T. Nakamura, Nuclear Instruments and Methods in Physics Research B **365**, 168 (2015).

[3] T. Narita, T. Kachi, K. Kataoka and T. Uesugi, Appl. Phys. Exp. **10**, 016501 (2017).

[4] K. Nishiguchi, S. Kaneki, S. Ozaki and T. Hashizume, Jpn. J. Appl. Phys. **56**, 101001 (2017).

[5] H. Hasegawa and H. Ohno, J. Vac. Sci. & Technol. B **4**, 1130 (1986).

[6] Y. Tokuda, Y. Matsuoka, H. Ueda, O. Ishigro, N. Soejima and T. Kachi, Superlattice and Microstructures **40**, 268 (2006).

[7] A. Uedono, S. Takashima, M. Edo, K. Ueno, H. Matsuyama, W. Egger, T. Koschine, C. Hugenschmidt, M. Dickmann, K. Kojima, S.F. Chichibu and S. Ishibashi, Phys. Status Solidi B **255**, 1700521 (2018).