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A Method for Accurate Extracting the Properties of Border Traps in Lateral GaN Power MOSFET with a Compact Distributed Network Model

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Abstract

The quality of gate dielectric is critical for GaN power MOS devices, while the trapping effect of the border traps close to the MOS interface could lead to reliability issues in those devices. In this paper, a compact model for border traps in lateral GaN MOS diode is proposed based on a distributed network of the border traps and channel resistance. Utilizing the limited response of border traps to ac signal, the modified model is used to profile energy and location dependent border trap density in GaN MOSFETs. We show that excluding the effect of channel resistance is critical for accurate calculating the distribution of border traps in lateral devices with low channel mobility, such as GaN MOS devices. The new insight derived from the impedance dispersion characteristics of lateral MOS devices is critical for quantitative analysis of the quality of III-V lateral MOS structures.

1. Introduction

The AlGaN/GaN high mobility transistor (HEMT) is widely studied as a promising candidate for high power electronic applications. For power switch applications, enhancement mode (E-Mode) GaN MOSFET utilizing gate recess combined with high quality high-k gate insulators deposited by atomic layer deposition (ALD) is applicable due to its large gate swing and low gate leakage current. In such devices, reliable dielectric with low trapping effect is highly desired for good channel transport property and long term reliability. Generally, the border traps located in the oxide layer close to the interface would give rise to reliability issues in these power devices. The properties of border trap is a key parameter to evaluate the quality of gate dielectric. Impedance measurement is a powerful tool to get an insight into the band diagram and charge distribution of the MOS devices. The frequency dependent impedance of lateral MOS devices contains abundant information including the trapping effects and channel resistance. Both these effects would induce the impedance frequency dispersion [1]. The impedance measurement is often conducted near the subthreshold region when the channel carrier density is low. The channel resistance is too high to be ignored in the lateral MOS capacitors especially for devices with low channel mobility, such as GaN MOS devices. Accurate modelling of these devices is critical for extracting the properties of traps and evaluating the quality of the MOS structure. Such modelling remains unavailable to this date.

In this letter, a model including the effects of the border traps and channel resistance is proposed. Utilizing the limited response of border traps to ac signal, the energy and location dependent distribution of border trap is extracted based on the compact model.

2. Result and Discussions

The lateral MOS diode as shown in Fig.1 (a) is a common test pattern compatible with the fabrication process of lateral FETs. The details of the fabrication process can be found in our previous work [2]. The channel sheet resistance calculated from the transfer curve is shown in Fig. 1(b). The measured impedance frequency dispersion of GaN lateral MOS structure is shown in Fig. 2(a) and (b). In the impedance measurement of lateral MOS structure, the high channel resistance would also give rise to the frequency dispersion since the ac signal would decay along the channel. The border trap density in the dielectric would be overestimated if one merely attribute the dispersion to border traps.

It is generally recognized that the border traps is distributed through the insulator. The charges in the channel interact with the border traps with a time constant. The time constant would scale with the distance from the interface. The trapping effect of distributed border traps in insulator can be represented by distributed network of *RC* circuit proposed by Yuan *et al*. [1]. The border traps with time constant τ larger than $1/f$ would not likely respond to the ac signal and therefore have

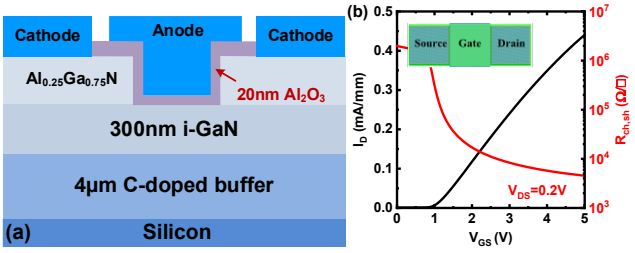

Fig. 1 (a) Schematic cross section of the Al_2O_3/GaN MOS diode. (b) Transfer curve and the extracted channel resistance of a GaN FAT-FET with L_G=100μm.

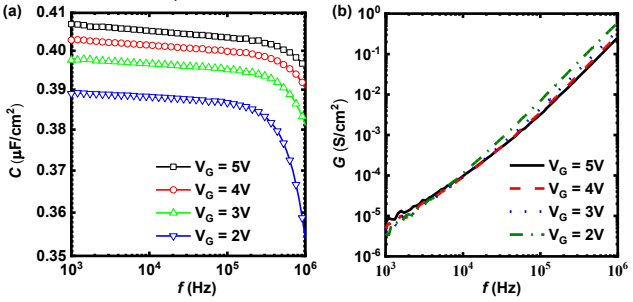

Fig. 2. Measured (a) C-*f* and (b) G-*f* curves of the gate MOS diode in the normally-off Al_2O_3/GaN FAT-FET.

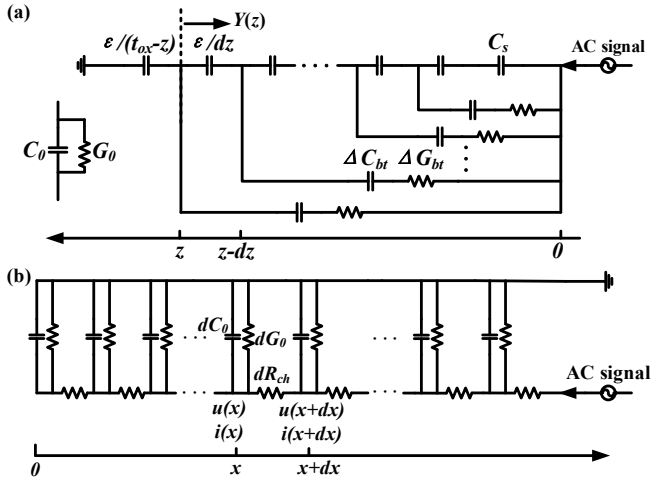

Fig. 3. (a) Modified equivalent circuit for bulk-oxide traps distributed over the depth of the insulator, assuming the one far from the interface would not response to a certain frequency. (b) Equivalent circuit model of gate region in the lateral Al_2O_3/GaN MOSFET.

little influence on the impedance dispersion. The distributed border trap model then can be modified as shown in Fig. 3(a). Supposing border traps located at position farther than $z = -\lambda \ln(f\tau_0)$ from the interface could not response to the ac signal with frequency *f*, the equivalent admittance at a point *z* in Fig. 3(a) is $\frac{1}{Y(z)} = \frac{1}{G_0 + j\omega C_0} - \frac{t_{ox}-z}{j\omega\varepsilon}$. Then the impedance frequency relation can be simplified as,

$$\frac{dC(z)}{dz} = \frac{G^2-\omega^2C^2}{\omega^2\varepsilon} + A\frac{q^2N_{ot}}{2\pi},\ A = 1.41 \quad (1)$$

$$\frac{dG(z)}{dz} = -\frac{2GC}{\varepsilon} + Bq^2N_{ot},\ B = 1.8504 \quad (2)$$

The separation of capacitance and conductance make it possible to minimize the effect of leakage current of the insulator layer.

The channel resistance complicates the extraction process of border trap properties from the experimental results. Excluding the effect of channel resistance is critical to get the insight into the trapping effect of border traps. In order to correctly model the lateral MOS capacitor for border trap property evaluation, an equivalent circuit for the lateral capacitor is proposed as shown in Fig. 3(b), consisting of the differential capacitance dC_0, the differential conductance dG_0 and the differential channel resistance dR_{ch}. The total admittance of the capacitor is then given according to the transmission line model,

$$Y = \frac{2W(\alpha+j\beta)}{R_{ch}} \frac{e^{(\alpha+j\beta)L}-1}{e^{(\alpha+j\beta)L}+1} \quad (3)$$

where $\alpha^2 = \frac{R_{ch}G_0 + \sqrt{(R_{ch}G_0)^2+\omega^2C_0^2R_{ch}^2}}{2}$, $\beta = \frac{\omega C_0 R_{ch}}{2\alpha}$. The total admittance seen by the gate is $Y = G_m + j\omega C_m$. G_0 and C_0 can be obtained by analytically solve Eq. (3) used for the boundary condition of Eq. (1). The modified model transforming the variable differential equation into the algebraic equations [Eq. (1) and (2)] is necessary to get a deeper insight into the characteristics of border traps, such as the depth distribution. Fig. 5(a) shows the detailed procedure to extract the spatial distribution of the border traps. Fig. 4(a) and (b) show the intermediate results during the calculation, in which C_0 and G_0 are the equivalent impedance values of the MOS structure only including the effect of the border traps. The difference between solid lines and dash lines in Fig. 4(a) and (b) reveals the importance of excluding the effect of channel resistance. Fig. 5(b) shows the spatial and energy dependent distribution of the border traps according to the modified model. The border traps locate mainly near the interface, which has been proved previously based on the low frequency noise and ac-g_m measurement data, suggesting the validity of the modified model.

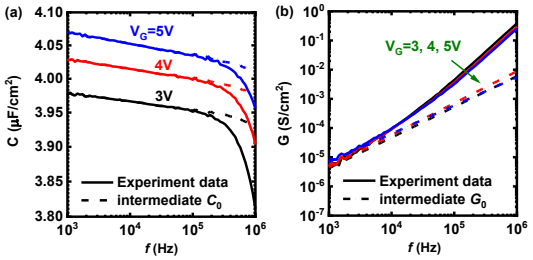

Fig. 4 (a) *C*(*f*) and (b) *G*(*f*) dispersion curves of the Al_2O_3/GaN MOS diode measured with different gate bias. The intermediate parameter C_0 and G_0 purely related to the border traps are also shown by excluding the effect of distributed channel resistance.

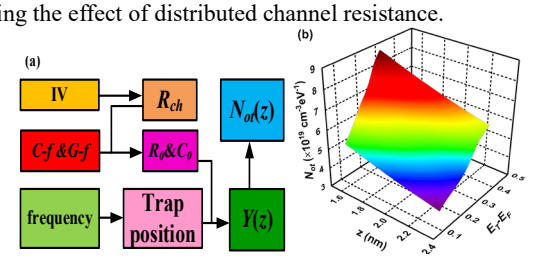

Fig. 5 (a) The detailed procedure to extract trap distribution in position and energy from C-*f* and G-*f* dispersion data. (b) The spatial and energy distribution of border traps in the Al_2O_3/GaN MOS structure extracted by the proposed compact model.

3. Conclusions

A compact model including the effects of both border traps and channel resistance perfectly depicts the measured *C-f* and *G-f* curves of the lateral Al_2O_3/GaN capacitors in a gate recessed normally-off GaN MOSFET. The proposed model is applicable for the MOS structure devices biased in the accumulation region with large channel resistance. Using the limited response of border traps to the high frequency ac signals, the compact model is used to profile the depth and energy dependent density of the border traps in the GaN MOSFETs. The proposed model is also applicable for other semiconductor devices with a high channel resistance, including ones with low channel mobility and low carrier density when biased near the threshold voltage

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References

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