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Demonstration of n-MOSFET operation and internal charge analysis of SiO_2/Al_2O_3 gate dielectric on (111) oriented 3C-SiC

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Abstract

We fabricated n-MOSFET with SiO_2/Al_2O_3 gate dielectric on (111) oriented 3C-SiC substrate. Fabricated device operated as inversion mode MOSFET successfully. We also analyzed fixed charge and interfacial dipole of SiO_2/Al_2O_3 gate dielectric on (111) n-type 3C-SiC. Both the SiO_2 and Al_2O_3 have negative fixed charge and the gate stack includes large dipole which shifts flatband voltage to negative direction. These results may open a way for application of 3C-SiC electronic device.

1. Introduction

Silicon carbide (SiC) has been attracting much interest as a material for high efficient and small size power devices due to its high breakdown field. Among some polytypes of SiC, (111) oriented 3C-SiC can be grown on Si (111) surface [1]. Therefore, 3C-SiC/Si hetero-epitaxial substrate has a potential for on-chip hetero-integrated electronic device. In order to apply high feasibility of 3C-SiC for electronic devices, it is necessary to form good dielectric on 3C-SiC with high interfacial quality for MOS gate and surface passivation layer. We have succeeded fabrication of 3C-SiC MOS capacitor with high interfacial quality (interface state density: $D_{it} < 10^{11}$ cm^{-2}eV^{-1}) by using SiO_2/Al_2O_3 stacked gate dielectric (Fig. 1) [2]. The MOS capacitor showed slightly negative flatband voltage (V_{fb}). In order to switch MOSFET by appropriate supply voltage, the V_{fb} and threshold voltage control is important. Concerning layer stacked gate dielectric, fixed charge (Q_{fix}) in each layer and interface dipole (δ_{dipole}) influence V_{fb}. In this article, firstly we demonstrated operation of 3C-SiC n-MOSFET with this gate dielectric. Secondly, we investigated Q_{fix} and δ_{dipole} in SiO_2/Al_2O_3 dielectric on 3C-SiC in anticipation of V_{th} control.

2. 3C-SiC n-MOSFET operation

The substrate used for n-MOSFET was (111) oriented p-type 3C-SiC epitaxially grown on p-Si (111) substrate. Hole concentration of 3C-SiC is on the order of 10^{16} cm^{-3}. Fabrication overview is summarized in Fig. 2. Source/drain (S/D) region was formed by multistep ion implantation of P (30-180 keV) and subsequent activation annealing at 1200°C. The gate stack was formed by the same method with our former study [2]. After substrate cleaning, Al_2O_3 by ALD and SiO_2 by ECR plasma sputtering were deposited as a gate dielectric. Next, post deposition annealing (PDA) was performed at 500°C in N_2 ambient. Al electrode was formed by thermal evaporation, and it was patterned for gate electrode by lithography and wet etching.

Figures 3(a) and 3(b) show I_D-V_D and I_D-V_G characteristics of the fabricated MOSFET, respectively. They showed typical MOSFET operation curve, thus the SiO_2/Al_2O_3 gate dielectric successfully controlled inversion carrier. However, leakage current at S/D junction is large. S/D formation by ion implantation must be optimized in the next step.

3. Fixed charge (Q_{fix}), interface dipole (δ_{dipole}) analysis

The substrate used for charge analysis in the gate stack was (111) oriented n-type 3C-SiC epitaxially grown on n-Si (111) substrate. Donor (nitrogen) concentration of 3C-SiC is on the order of 10^{16} cm^{-3}. In this study, we fabricated lateral MOS capacitors and the fabrication detail is the same with MOSFET fabrication. In Fig. 4, the principle of Q_{fix} and δ_{dipole} evaluation is illustrated. If non-mobile charges in the gate stack are centralized at interfaces and bulk charges can be negligible, V_{fb} can be expressed by the equation (1) in Fig. 4 and V_{fb}-EOT plot shows liner relationship [3]. By changing SiO_2 thickness (EOT_1) and Al_2O_3 thickness (EOT_2), we can evaluate Q_{fix1} and Q_{fix2} from the slope of V_{fb}-EOT_1 and V_{fb}-EOT_2 plot. Vertical intercept corresponds δ_{dipole}.

Figure 5(b) shows high frequency (100 kHz) *C*-*V* characteristics for samples with various Al_2O_3 thickness. Typical n-type *C*-*V* curves were obtained for all samples, and V_{fb} shifts to positive direction with increasing EOT. V_{fb}-EOT_2 plots for these samples are summarized in Fig. 5(c). It shows good liner relationship which means the effect of bulk charges are weak. Q_{fix2} located at Al_2O_3/SiC interface are obtained as -2.77×10^{11} cm^{-2} from the slope. Similarly, *C*-*V* characteristics and V_{FB}-EOT_1 plot for the samples with various SiO_2 thickness are shown in Figs. 6(b) and 6(c), respectively. From the slope of Fig. 6(c) and Q_{fix2}, Q_{fix1} located at SiO_2/Al_2O_3 interface was obtained as -5.96×10^{11} cm^{-2}. By using workfunctions of 3C-SiC (4.21 eV) [4] and Al (4.08 eV), δ_{dipole} is calculated as -0.99 eV. Analyzed charge distribution is illustrated in Fig. 7. Since the dipole strength is relatively large, material (especially gate electrode) and process should be well designed for device application.

4. Conclusions

We demonstrated operation of n-MOSFET with SiO_2/Al_2O_3 gate dielectric on (111) oriented 3C-SiC. We also analyzed internal charge of the same gate dielectric. The SiO_2 and Al_2O_3 have negative Q_{fix}, and the gate stack includes large dipole of -0.99 eV. This large dipole should be considered for device application.

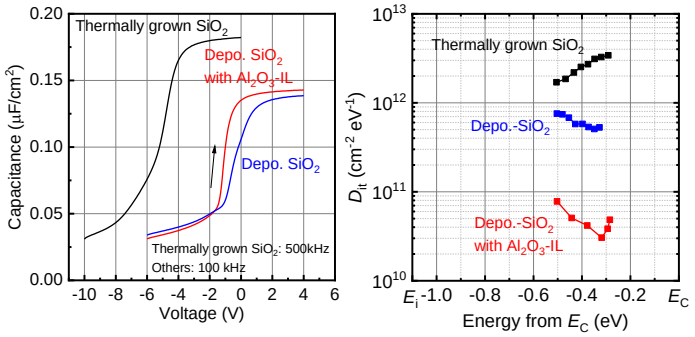


Fig. 1 (a) *C-V* characteristics and (b) D_{it} distributions for 3C-SiC MOS capacitors with various structures [2].

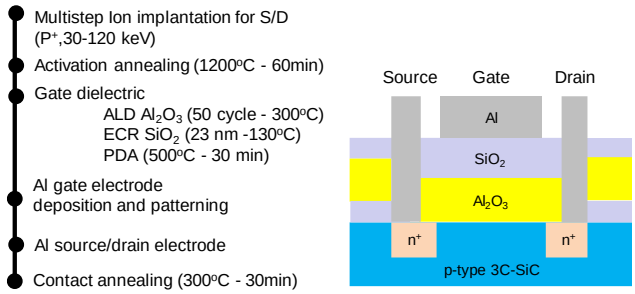


Fig. 2 Fabrication procedure and cross sectional illustration of 3C-SiC n-MOSFET.

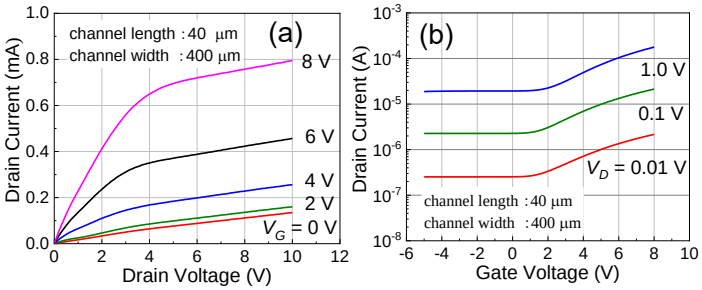


Fig. 3 (a) I_D-V_D and (b) I_D-V_G characteristics of fabricated 3C-SiC n-MOSFET with SiO_2/Al_2O_3 gate dielectric.

$$V_{fb} = \Phi_M - \Phi_S + \delta_{dipole} - \frac{Q_{fix2}}{\varepsilon_0 \varepsilon_{SiO_2}}(EOT_1 + EOT_2) - \frac{Q_{fix1}}{\varepsilon_0 \varepsilon_{SiO_2}} EOT_1 \quad \ldots(1)$$

Φ_M, Φ_S: workfunction of the gate electrode and the semiconductor
Δ_{dipole}: total dipole in the gate stack
Q_{fix1}, EOT_1: fixed charge and EOT of the top gate dielectric
Q_{fix2}, EOT_2: fixed charge and EOT of the bottom gate dielectric
ε_{SiO2}: SiO_2 dielectric constant
(EOT: equivalent oxide thickness)

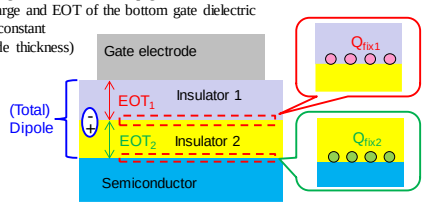
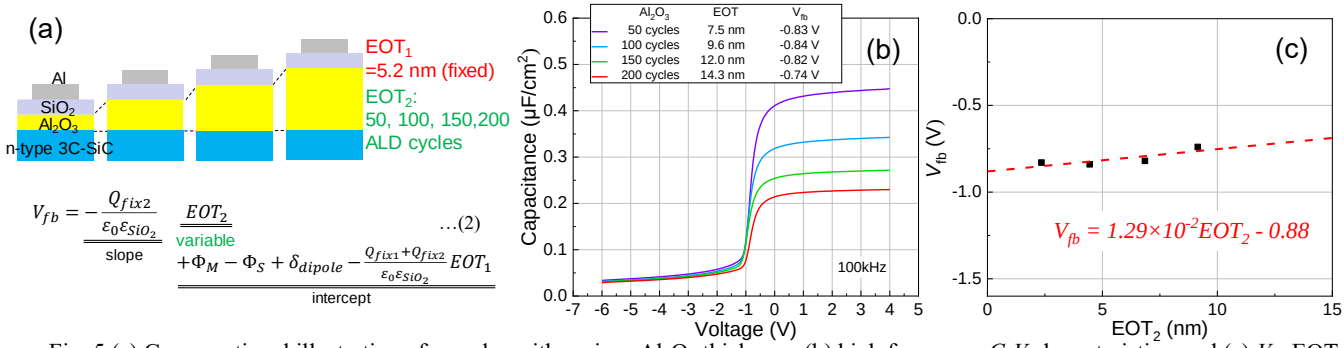
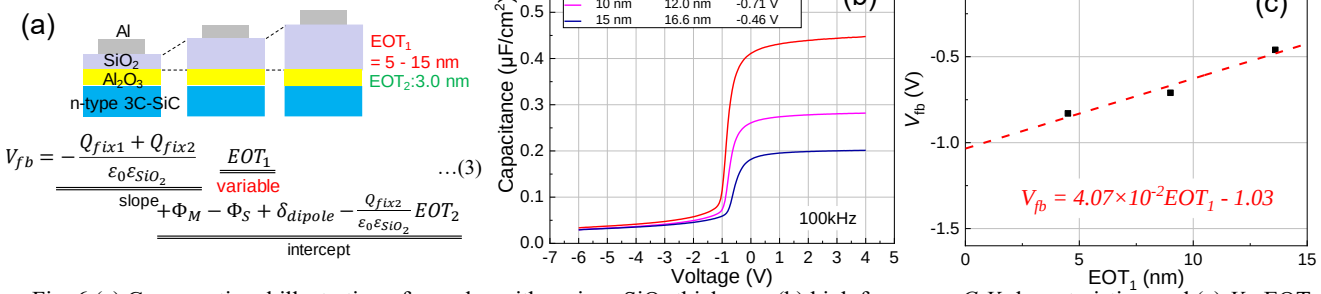


Fig. 4 Sample cross-sectional illustration and V_{FB} equation.



$$V_{fb} = -\frac{Q_{fix2}}{\varepsilon_0 \varepsilon_{SiO_2}} \underbrace{\frac{EOT_2}{\text{variable}}}_{\text{slope}} + \underbrace{\Phi_M - \Phi_S + \delta_{dipole} - \frac{Q_{fix1}+Q_{fix2}}{\varepsilon_0 \varepsilon_{SiO_2}} EOT_1}_{\text{intercept}} \quad \ldots(2)$$

Fig. 5 (a) Cross sectional illustration of samples with various Al_2O_3 thickness, (b) high frequency *C-V* characteristics, and (c) V_{fb}-EOT_2 plot for Q_{fix2} and δ_{dipole} estimation.



$$V_{fb} = -\underbrace{\frac{Q_{fix1} + Q_{fix2}}{\varepsilon_0 \varepsilon_{SiO_2}}}_{\text{slope}} \underbrace{\frac{EOT_1}{\text{variable}}}_{} + \underbrace{\Phi_M - \Phi_S + \delta_{dipole} - \frac{Q_{fix2}}{\varepsilon_0 \varepsilon_{SiO_2}} EOT_2}_{\text{intercept}} \quad \ldots(3)$$

Fig. 6 (a) Cross sectional illustration of samples with various SiO_2 thickness, (b) high frequency *C-V* characteristics, and (c) V_{fb}-EOT_1 plot for Q_{fix1} estimation.

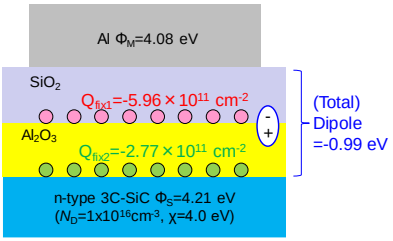


Fig. 7 Analyzed charge distribution in this study.

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References

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