

# 1T Semi-floating Gate Image Sensor with Enhanced Quantum Efficiency and High Response Speed

Zi-Ling Tian<sup>1</sup>, Chen-Xi Yue<sup>1</sup>, Chen Wang<sup>1</sup>, Lin Chen<sup>1\*</sup>, Hao Zhu<sup>1</sup>, Qing-Qing Sun<sup>1</sup>, and David Wei Zhang<sup>1</sup>

<sup>1</sup>State Key Lab. of ASIC and System, School of Microelectronics, Fudan University, Shanghai, 200433, China

Phone: +86-21-55664609 \*E-mail: [linchen@fudan.edu.cn](mailto:linchen@fudan.edu.cn)

## Abstract

The active pixel image sensor based on semi-floating gate transistor (SFGT-APS) has been proposed and investigated; however, the quantum efficiency and the sensitivity are too poor to meet low illumination intensity and high-speed application due to the shallow junction of photodiodes. In this work, we demonstrate a new structure, called buried photodiode semi-floating gate transistor active pixel image sensor (BSFGT-APS), which possesses enhanced quantum efficiency, high sensitivity, and fast response speed. Moreover, BSFGT-APS has the same fill factor with SFGT-APS, which is 55% with a  $1\ \mu\text{m}^2$  photodiode in  $0.13\ \mu\text{m}$  process. The basic device characteristics were investigated by Sentaurus TCAD simulation, including transient response, dark current, conversion gain, and full well capacity.

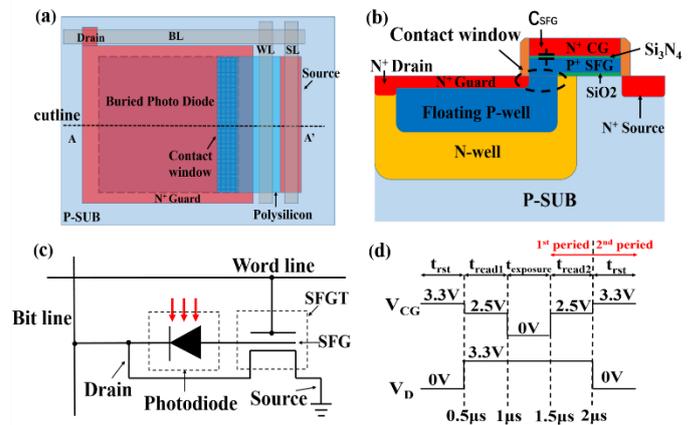
## 1. Introduction

In the past few years, the active pixel image sensor based on semi-floating gate transistor (SFGT-APS) has been proposed[1]-[2] and investigated [3]. It has a higher fill factor and a higher pixel density with a simple 1T active pixel structure and can realize the functions of the conventional 3T CMOS image sensor[4]-[5]. However, due to the shallow junction of photodiodes, the quantum efficiency and sensitivity are too poor to meet low illumination intensity and high-speed application. In addition, the manufacturing process is incompatible with self-aligned technology since the drain is covered by a polysilicon gate and extra masking steps are necessary, which increases complexity and cost. In this paper, a new structure, called buried photodiode semi-floating gate transistor active pixel image sensor (BSFGT-APS), is proposed. Compared with SFGT-APS, this structure contains a large and deep floating P-well in the photodiode, and an additional narrow N+ guard layer is deposited on the floating P-well to expand the depletion region of the photodiode. The characterization of this structure was investigated through Sentaurus TCAD simulation. Our simulation results indicated that the quantum efficiency was reinforced and the overall response speed was promoted. Furthermore, transient response, dark current, conversion gain, and full well capacity were also investigated for this paper.

## 2. Device Structure and Principle

The plan view and cross-sectional view of BSFGT-APS are shown in Fig. 1(a) and Fig. 1 (b), respectively. The photodiode located at left side is formed by the floating P-well surrounded by deep N-well, and additional narrow N+ guard layer is deposited on the floating P-well. The SFGT located at right side contains the P+ doped polysilicon semi-floating

gate(SFG) and the N+ doped polysilicon control gate(CG). There is a contact window on the side of the first SiO<sub>2</sub> dielectric layer, through which the floating P-well is directly contacted with the SFG. The second dielectric layer between CG and SFG is Si<sub>3</sub>N<sub>4</sub>. Fig. 1(c) shows the equivalent schematic diagram of a BSFGT-APS. The bit line is connected to the drain electrode, hence the drain current is read out as output signal. The CG electrode is attached to word line as a switch. The BSFGT-APS uses the holes as signal charges and SFG as a charge storage capacitor(C<sub>SFG</sub>). Through collecting or eliminating the photo-generated holes in SFG region, the threshold voltage(V<sub>th</sub>) of SFGT can be modulated. Then the drain current as output signal is changed with different V<sub>th</sub>. Additionally, due to the floating P-well is surrounded by N-well, photo-generated holes inside the floating P-well are confined in it, and the electrical crosstalk between the neighboring cells will be reduced.



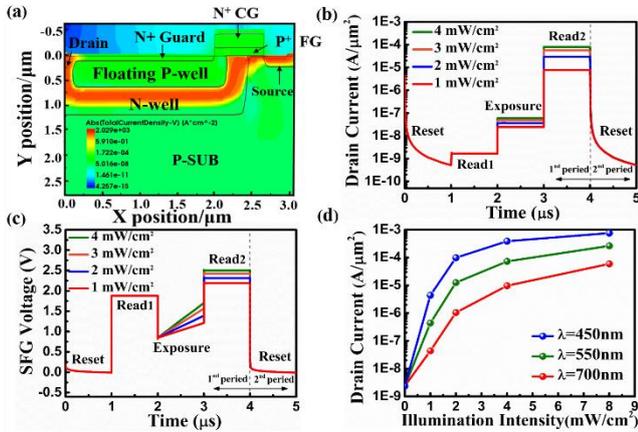
**Fig. 1** The plan view (a) of BSFGT-APS and the cross sectional view along the cutline AA'(b). The equivalent schematic diagram of BSFGT-APS (c). The time sequence and the voltage setting for every operation(d).

## 3. Results and Discussion

In order to investigate the performance of the BSFGT-APS, 2-dimensional Sentaurus TCAD simulation is performed. The time sequence and the voltage setting for every operation are shown in Fig. 1(d). There are four phases in one operation cycle, consisting of reset, read1, exposure and read2. The duration time of each operation is  $1\ \mu\text{s}$  and the source and substrate electrode are always connected to ground.

The transient simulations are as followed: Firstly, the reset operation is achieved with drain voltage( $V_D$ ) of 0 V and control-gate voltage( $V_{CG}$ ) of 3.3 V. Since the N well is connected to the SFGT's drain, the buried photodiode is operated in forward biased state. the stored holes in SFG are pushed away

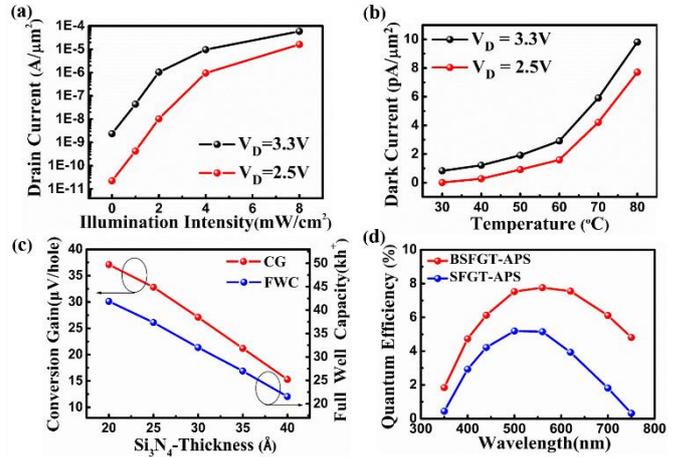
through the contact window and the floating p-well is refreshed and initialized. Then in the read1 phase,  $V_{CG}$  and  $V_D$  are set to 2.5 V and 3.3 V, respectively, The SFG voltage rises to a certain value due to the increased control-gate voltage. Then the SFGT is turned on and the drain current is read out as the first signal of the double sampling. After the read1 phase,  $V_{CG}$  is changed to 0 V and the  $V_D$  is remained 3.3 V, the BSFGT- APS is entered into the exposure phase. Photo-generation holes will be driven to SFG through the contact window under the reverse-biased electronic field, leading to decreased the  $V_{th}$ . The illumination intensity and the exposure time determine the variable of the  $V_{th}$ . Finally, in the read2 phase, the voltage setting is same as the read1 phase., and the reduction of the  $V_{th}$  in the exposure phase results in the amplify of the drain current, which is read out as the second signal of the double sampling. The contour of the total current density in read2 phase is shown in Fig. 2(a). The difference between first and second readout signal is the effect of illumination, which is to be calculated by correlated double sampling (CDS) circuit to eliminate flat pattern noise (FPN). The transient response of the drain current varying with time is shown in Fig. 2(b). Meanwhile, the drain current in exposure phase is a bit larger than that of SFGT-APS because of the large photocurrent, leading to accelerate the charging of the  $C_{SFG}$ . Fig. 2(c) shows the transient response of SFG voltage ( $V_{SFG}$ ) versus time with different light intensities.



**Fig. 2** The transient response of the drain current varying with time under 1mW/cm<sup>2</sup>, 2 mW/cm<sup>2</sup>, 3 mW/cm<sup>2</sup>, and 4 mW/cm<sup>2</sup> illumination intensities in 550nm wavelength(a). The transient response of the SFG voltage varying with time under 1 mW/cm<sup>2</sup>, 2 mW/cm<sup>2</sup>, 3 mW/cm<sup>2</sup>, and 4 mW/cm<sup>2</sup> illumination intensities in 550nm wavelength(b). The contour of the total current density in read2 phase(c). The drain current varies with illumination intensities in 700nm, 550nm and 450nm wavelengths(d).

The drain current as the output signal is mainly impacted by illumination intensity and drain voltage, so the relationship between drain current and illumination intensity under different wavelengths is investigated in Fig. 2(d). The simulation results for drain current versus illumination intensity under different drain voltages are also extracted in Fig. 3(a). The dark current is an important parameter for image sensor, which is able to influence the dynamic range and noise. So the dark current value has been studied by the TCAD simulation in Fig. 3(b). Full well capacity(FWC) and conversion

gain(CG) as basic parameters of image sensor are also investigated in Fig. 3(c). Both of them are closely connected with the  $C_{SFG}$ , which is determined by the ratio of dielectric constant to the thickness of Si<sub>3</sub>N<sub>4</sub> dielectric layer. The quantum efficiency(QE) is defined as ratio of the number of photo-generated holes to the number of input photons on a pixel, which is simulated corresponding to different wavelength in Fig. 3(d).



**Fig. 3** The drain current varies with illumination intensity in 2.5 V and 3.3 V drain voltage(a). The dark current varies with temperature in 2.5 V and 3.3 V drain voltage(b). Full well capacity(FWC) and conversion gain(CG) vary with the thickness of Si<sub>3</sub>N<sub>4</sub> dielectric layer(c). Quantum efficiency varies with wavelengths in visible spectrum corresponding to SFGT-APS and BSFGT-APS.

#### 4. Conclusions

In this paper, we introduced the structure and the performance of the BSFG-APS. Based on the results of the simulation, we can come to the conclusion that compared with the SFG-APS, the BSFG-APS not only has the same fill factor but also possesses the enhanced quantum efficiency, high sensitivity and fast response speed. The whole operation period is remarkably reduced and can be achieved in the microsecond level, resulting in the feasibility for high-speed application. We believe that such a high-performance image sensor is very promising for high-density and high-speed applications in the future.

#### Acknowledgement

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