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Impact of Heat Guide Thickness on Output Power of Planar Silicon Thermoelectric Generator

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Abstract

We investigate the impact of the thickness of a heat guide (HG) layer on the thermoelectric (TE) power of a cavity-free planar micro TE generator (μ-TEG) using Si nanowires (Si-NWs). The TE power is enhanced by placing a thick metal layer on the hot side electrode, which act as the HG into the μ-TEG. There is a trade-off thickness between the that of the HG and the separation from the cold-side electrode surface, so that an optimum thickness exists for maximizing the TE power. The optimum thickness depends on the insulating materials filling the space between cold-side electrodes and the heat source plate hanging over the TEG device. The results clarify the importance of the backend engineering in enhancing the performance of the μ-TEGs.

1. Introduction

Towards the IoT era, TE power generation is attracting many attentions as a perpetual power source to drive distributed sensor nodes. Especially, high expectations are placed on the silicon-based μ-TEGs which will be manufacturable with the current CMOS process,[1,2] ever since the discovery of superior TE property of silicon nanowires(Si-NWs) [3].

Our research group proposed a new μ-TEG architecture in which Si-NWs lie on the insulating oxide surface without forming a cavity structure underneath them [4,5] (Fig.1). The μ-TEG is driven by injecting heat energy perpendicular to the substrate through a HG layer [6]; a large heat source plate is placed on the TEG module, and the heat current exuded from the HG flows into Si-NWs. It is important to secure the temperature gradient in the Si-NWs, so that the thermal leakage from the heat source to the cold-side electrodes must be suppressed by increasing the height of HG layer. On the other hand, the thermal resistance at the HG increases with the thickness, thereby most of the heat energy is dissipated in the thick HG layer and the temperature difference in Si-NWs decreases. In this study, we engineered the HG structure to maximize the TE performance of our proposed device.

2. Experimental

Fig. 2 shows a sectional view of the fabricated μ-TEG. The μ-TEG is composed of 400 Si-NWs, Si pads, metal electrodes, and Al HG film. The lengths of the Si-NW L_{NW} are $18\ \mu$m and $100\ \mu$m. The width of the Si-NW is 100 nm.

Fig. 3 shows the fabrication procedure of the μ-TEG with HG layer. The μ-TEG is fabricated on an SOI substrate (SOI:88nm, BOX:145nm, Si substrate:745μm). First, the SOI layer was patterned into Si-NWs and Si pads. Then, P+ ions were implanted ($1.0\times10^{15}\mathrm{cm}^{-2}, 25\mathrm{keV}$) and activation annealing was performed. Next, TiN/Al/TiN/Ti (30nm/400nm/30nm/10nm) electrodes was deposited on the Si pads. Finally, $0.5\ \mu$m and $1\ \mu$m of Al HG layer was deposited on the hot side electrode. In TE measurements, a micro heat source heated at $318\mathrm{K}$ placed over the μ-TEG. The micro heat source is made of AlN ceramics plate and its bottom surface is contacted with the Al HG. The sample stage is cooled at $293\mathrm{K}$ by a Peltier cooler.

3. Results and Discussion

Fig. 4 shows the open circuit voltage V_{oc} for different thicknesses of Al HG layer. V_{oc} is successfully enhanced by increasing the HG layer thickness. The heat conduction from the heat source plate, which hangs over the specimen, to the cold-side electrode is more suppressed by increasing the HG layer height, and the temperature difference across Si-NWs is secured furthermore.

Fig. 5 shows the simulation result in the case that the interlayer space is filled by the air. The V_{oc} is enhanced as the HG thickness increases when the thickness is less than 1μm. However, the V_{oc} turns to decrease when the HG thickness exceeds 3μm, where the thick HG layer impedes the heat flow injected from the heat source plate. The optimum HG thickness for the case L_{NW}=18μm is thinner than that of the case of L_{NW}=100μm. In both cases, more than 1μm thick of the HG layer is required to obtain an enough Voc.

In the practical implementation of the planar μ-TEG, it will be embedded in SiO_2 interlayer as well as other CMOS devices. The HG to the hot-side electrode is fabricated by filling a metal into a contact hole in the SiO_2 layer (Fig.6).

The simulation result shows that the V_{oc} decreases by replacing the open space filled with air to SiO_2 (Fig. 7), and more than 10µm thick HG layer is required to maximize Voc. This is because SiO_2 has a higher thermal conductivity (1.4 W/m·K) than that of the air (0.026 W/m·K) Large V_{oc} can be maintained if we employ a porous silica with low thermal conductivity of 0.2 W/m·K.[7]. Since the porous silica has been used in the CMOS devices as a low-k insulator, it is a practical material to fill the interlayer space of HG to realize the high performance of TEG.

4. Conclusions

We investigated the optimum height of the Al HG layer deposited on cavity-free planar-type Si-NW µ-TEG. We experimentally confirmed that V_{oc} enhanced with increasing Al layer height. The optimum Al height is numerically expected more than 1µm.

The planar µ-TEG will be embedded in SiO_2 interlayer in the practical implementation. Even in that case, high V_{oc} can be maintained by employing the porous SiO_2.

Acknowledgements

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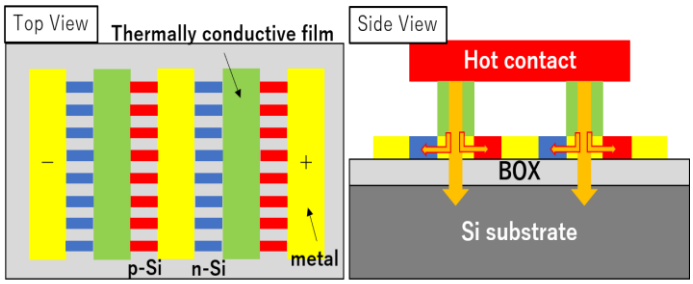

Fig.1 Schematic of the cavity-free planar-type µ-TEG.

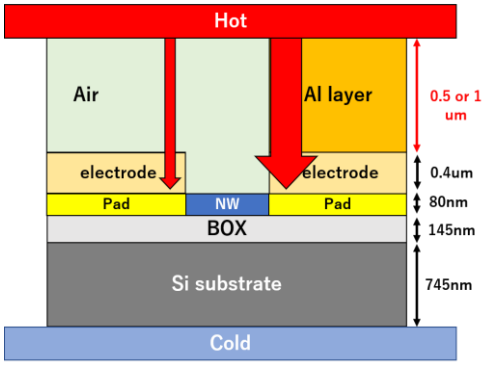

Fig.2 Sectional view of the µ-TEG.

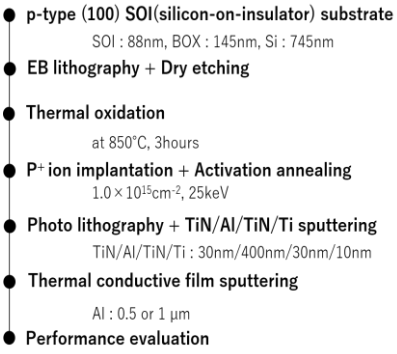

Fig.3 Process flow of the µ-TEG.

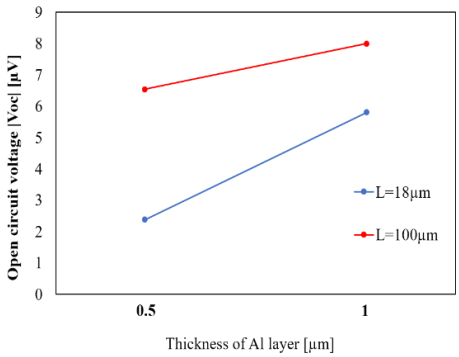

Fig.4 Thickness dependence of TE power of µ-TEG in air (experiment).

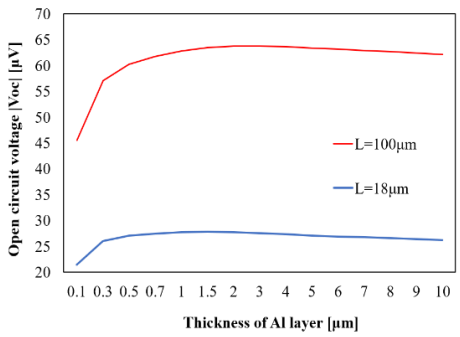

Fig.5 Thickness dependency of TE power of µ-TEG in air (simulation).

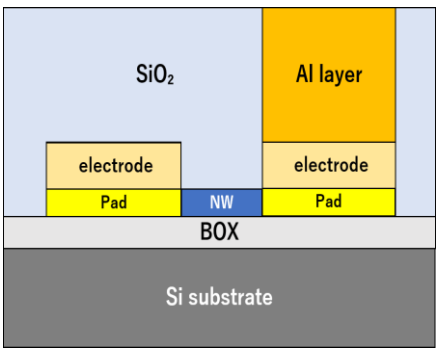

Fig.6 Sectional view of the µ-TEG embedded in SiO_2

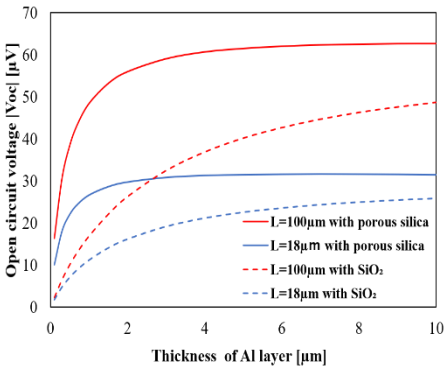

Fig.7 Thickness dependency of TE power of µ-TEG embedded in SiO_2 and porous silica (simulation)