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A MoS_2 channel-based Ferro- FET with charge trapping and switching effects

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Abstract

We present a Ferro-FET transistor based on the combination of two distinctive mechanisms, namely, polarization in ferroelectrics and charge trapping effects. Here, molybdenum disulfide (MoS_2) is used as the channel semiconductor. The as-deposited 15 nm hafnium zirconium oxide (HfZrO) film implemented as gate dielectric showed ferroelectricity. The charge trapping phenomenon in this device was explored by characterizing the transfer curves with different range of gate voltages. The transfer characteristic of this device was demonstrated with operating voltage that was smaller than 4V, high on-off current ratio about 10^6, and subthreshold slope (SS) less than 150mV/dec. The gate stack design and memory operation of the hybrid device are aimed to offer mutually benefits between the charge trapping and switching effects, which show good potential for memory systems and applications.

1. Introduction

Ferroelectric RAMs (FRAMs) are low-power, nonvolatile devices, but FRAM has not scaled beyond the 130nm technology node due to the fact that only planar capacitors can be used and the traditional ferroelectric films are not scalable[1]. Therefore, new class memory type transistors, challenges to develop a transistor with a scalable, embedded Fe-FET (ferroelectric FET) memory with low-power and nonvolatile properties are demanding. Ferroelectric memory writes an application using an electric field only and no current flow, which will meet the requirement of the new memories applications. Monolayer MoS_2 has relatively small dielectric constant and atomic thickness, which are promising candidates for channel material due to their immunity to short-channel effects (SCE) [2].

In our work, we proposed a CVD-grown monolayer MoS_2 based Ferro FET with HfZrO (HZO) ferroelectric layer as the gate dielectric. The device exhibits a very clear memory hysteresis. Subthreshold slope is less than 130 mV/dec, and a high on/off current ratio is more than 10^6. Typical current-voltage measurements were presented as evidence of ferroelectricity; trapping effects of interface between the HfO_2 and the MoS_2 channel layer were also demonstrated. As to retention property, two distinctive read and retention states were exhibited.

2. Experimental details

The process flow schematics for fabricating the device in this work are found in figure 1(a). Titanium nitride (TiN) was grown from Physical Vapor Deposition (PVD) on a SiO_2/p++ Si substrates. Following deposition of TiN, hafinium zirconium oxide (HZO) was grown using ALD (atomic layer deposition). HZO films were grown in a 1:1 Hf:Zr ratio and the TiN was grown on the HZO. TiN was patterned with photolithography and lift off to form gate. Then, 8nm hafnium oxide (HfO_2) was ALD-grown on them. CVD monolayer MoS_2 was transferred on the HfO_2 layer. Monolayer MoS_2 Flakes were optically characterized and thicknesses were confirmed with Raman, with flake thicknesses chosen ~0.3 nm for device. Followed by metallization with 50 nm Ti (contacts and leads) and 70 nm Au (contact pads), Lift-off was performed in 70°C heated acetone. Finally, the annealing process for the crystallization of device was performed by thermal annealing (250℃) in an Ar environment for 2 hours. The channel length of device is 10um and the width of device is 380um.

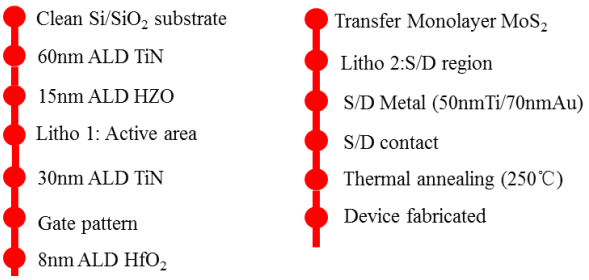

Fig. 1 The process flow schematics for fabricating the device

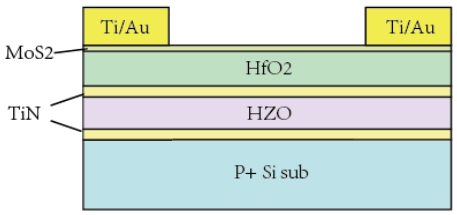

Fig. 2 Image of monolayer MoS_2-based Fe-FET transistor

3. Results and discussion

Before the characterization of MoS_2-based Fe-FET, the ferroelectric properties were investigated. Figure 3 show current-voltage characteristic of TiN/HZO/TiN structure, which were measured in air by using a semiconductor parameter analyzer (HP 4155, Agilent). The TiN/HZO/TiN layer exhibited typical ferroelectric behaviors.

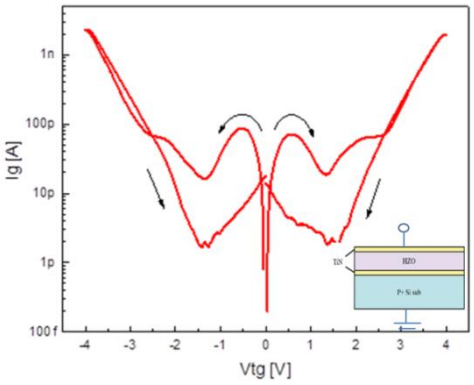

Fig. 3 Typical current-voltage (I-V) curve obtained from TiN/HZO/TiN structure

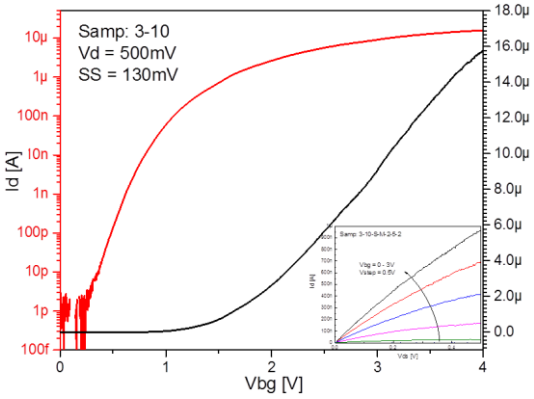

Fig. 4 Transfer characteristic and output characteristic of MoS_2 based Fe-FET

The transfer curves of the Fe-FET are shown in Figure 4. Subthreshold Swing (SS) is 130mV/dec and on/off current ratio is 10^6 at Vg ranging from 0V to 4V. The Ids-Vds output characteristics are presented in the inset of figure 4, which showing a good Ohmic contact between MoS_2 and Ti/Au metal.

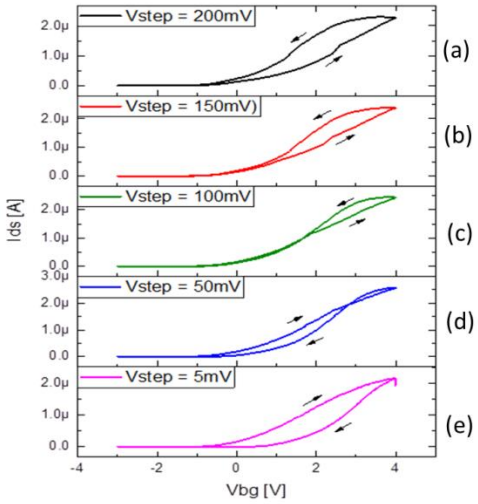

Fig.5 Sweeps of transfer curves of MoS_2-based Fe-FET with different sweeping steps of gate voltage

The transfer curves of the Fe-FET show typical counter-clockwise sweeping hysteresis due to ferroelectric polarization switching at drain voltages (V_d) of 0.5V for a Vg sweep step of 0.2V,0.15V and 0.1V, as shown in figure 5 (a-c). To analyze the charge trapping effect in this device, drain voltage of 0.5V for a Vg sweep step of 0.05V and 0.05V were applied as shown in figure 5(d-e). The clockwise hysteresis of Ids-Vg indicates that charge trapping (the interface between the HfO_2 and the MoS_2-channel layer) dominated. The variation of $\triangle V_T$ (less than 1V) is obtained from the same sample at room temperature. The variation of sweeping direction and $\triangle V_T$ in the device characteristics would be a concern owing to mutually benefits between the charge trapping and the switching effects.

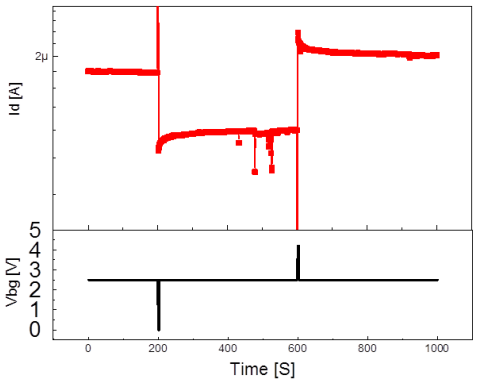

Fig.6 Pulse waveform and operational bias conditions for the MoS2-based Ferro-FET under a Vd of 0.5V

Memory operation is displayed with the timing versus bias in figure 6. The memory dynamic switching and static retention properties of MoS_2-based FE-FET were successfully demonstrated.

4. Conclusions

In summary, a MoS_2-based Fe-FET with HZO gate dielectric was presented. The as-deposited TiN/HZO/TiN film showed ferroelectricity according to the typical I-V measurements. We presented the MoS_2-based Fe-FET characteristic: on-off current ratio of about 10^6. And counterclockwise and clockwise sweep characteristics are demonstrated at room temperature with different sweeping steps of gate voltages. And two distinctive switching and retention states were exhibited.

Acknowledgements

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