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Sensitivity study on different gate dielectric dependence of DG-CNTFET using atomistic simulation NEGF approach

Chitra Pandy[1], V N Ramakrishnan[2] and Hidenori Mimura[1]
[1] Research Institute Electronics
Gradute School of Science and Technology,Shizuoka University, Johoku, 3-5-1,
Naka-ku, Hamamatus 432-8011, Japan
Phone: +090-9194-6249 E-mail: chitra.pandy.18@shizuoka.ac.jp
[2] VIT University, Vellore, Tamilnadu- 632014, India
Phone: +91-98-4095-4095

Abstract

This work reports the detailed study of the performance of DG-CNTFET taking into account of different dielectric in gate oxide materials. In this study, we have investigated the transfer characteristics, I_{ON}/I_{OFF} current ratio, subthreshold slope and Transconductance of the device using Non-Equilibrium Green Function (NEGF) formalism in atomistic level simulations. The output transfer characteristics of CNTFET is obtained by solving Schrodinger equation using NEGF which is self -consistently with 3D Poison's equation in NanoTCAD ViDEs and found its performance dependence on different dielectric material.

1. Introduction

The transistor is considered one of the greatest inventions of the past century. It has helped both the information and computing age to progress rapidly. One of the reasons for success is its ability to decrease in size and increase in speed. This property is summarized in Moore's law [1]. It derives that transistor's size will decrease exponentially while its speed increases exponentially. The physical barriers arise due to the continued shrinking of the current transistor used today such as the Metal-Oxide Field Effect Transistor or MOSFET. The MOSFET has become one of the most significant devices for the integrated circuits design application. In the field of semiconductor devices, continued success in device scaling is indispensable for further improvements. This scaling limits the serious issues in the fabrication process. The short channel effects, threshold voltage roll-off,high leakage current, and drain induced barrier lowering become increasingly significant as the channel length of the semiconductor device is reduced which makes less suitable for ultra-low power applications. The short channel effect and direct tunneling between source and drain limits the scaling capability of MOSFETs, when the channel length goes below 10 nm, silicon-based technology will start to reach its limits. Due to these limitations of MOSFETs, the semiconductor manufacturing is considering alternative materials and devices to integrate with the current silicon-based technology for upcoming development. The new promising Nano-devices, such as Silicon-On-Insulator (SOI) MOSFET, nanowire MOSFETs, FinFETs, TFET, JLFETs possess higher performance enhancements to reduce the device scaling complications. However, all these alternatives are not comparable with CNTFETs. The CNTFET can perform better in terms of both present and future technologies, despite the substantial Gate Length (L_g) and gate oxide thickness (t_{ox}). In the above-mentioned geometrical and process parameters, the CNTFET is one of the emerging technologies to supplement the current silicon-based MOSFET devices [2].

In this paper, we report different gate dielectric material dependence performance of the CNTFET with double gate structure. The output characteristics are obtained for different dielectric material self-consistently solving with Poisson's equation using NanoTCAD ViDES.

2. CNTFET Device

In the year 1991, Carbon Nano Tube (CNT) was introduced by Ijima, at the NEC Fundamental Research Laboratory in Tsukuba, Japan. CNT can be theoretically viewed as graphene single atomic layer of graphite sheets. It is rolled up into concentric cylinders. The atomic structure of a single-walled CNT can be easily expressed by two vectors namely chiral vector (ch) and Translational Vector (T). T is the direction of CNT axis and Ch indicates circumference which determines the diameter, bandgap and threshold voltage. The important property of CNTs is that they exhibit metallic as well as semiconducting. Chiral (n, m) determines this property that if (n-m) is divisible by 3, tube is metallic else semiconducting. The structure of CNTFET is grouped into two categories: Planar and coaxial. Planar type is most fabricated CNTFET type because of their simplicity and compatible with existing technologies. But coaxial is more preferred due to maximizing the capacitive coupling between gate and CNT surface [3]. In our work, double gate planar geometry is preferred for simulation.

2.1 Device Structure

A double gate device structure used in our simulation is shown in Fig 1. The CNT used with chirality of (7, 0) zig zag semiconducting type as a channel. Drain and source are extension of the channel doped with n type which is a conventional type CNTFET. Gate insulator is extended over source and drain. Device dimension parameters are given in Table -I.

Table -I Device Dimension

Parameter	Dimension
CNT Channel Length	5 nm
S/D length	5 nm
Dielectric	1 nm
Diameter	0.54 nm

Band gap	1.48 eV
Doping density (f)	5×10^{-3}

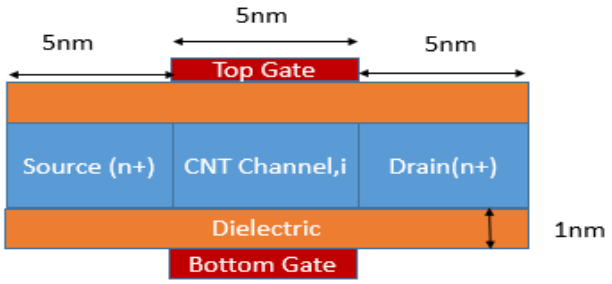

Fig 1. DG CNTFET Device structure

2.2 Simulation Approach

The output transfer characteristics of CNTFET is obtained by solving Schrodinger equation using NEGF which is self-consistently with 3D Poison's equation. Using this method, the current is computed by

$$I_d = \frac{4q}{h}\int_{-\infty}^{\infty} T(E)\left[f(E-\varepsilon_S)-f(E-\varepsilon_D)\right]dE \quad (1)$$

H is Plank's constant and T(E) is the transmission coefficient which is calculated using Green's function.

2.3 Simulation of I-V Characteristics

CNT is used for low power applications because of its low value off current. Simulations are performed by taking V_{DS} is constant as 0.1 V and 0.5 V and by varying V_{GS} from 0 V to 1 V. The Current-Voltage transfer characteristics of DG-CNTFET is shown in Fig 2.

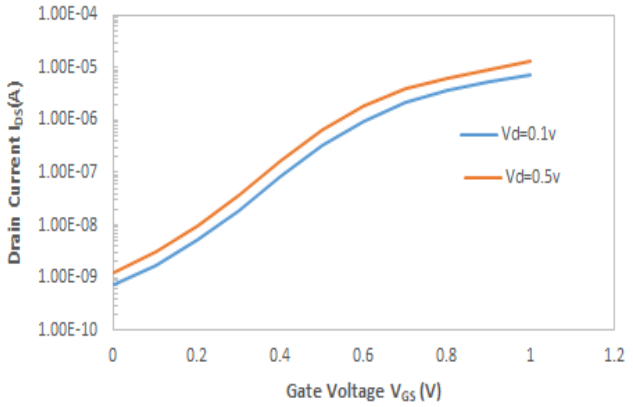

Fig 2. I_{DS}-V_{GS} Characteristics for Different V_{DS}

It offers low I_{OFF} current in the order of 10^{-10} due to the enhancement mode operation of the device suitable for low power applications. I_{ON} is high due to the doping concentration of source and drain.

2.4 Effect of Different Dielectric materials

A high quality high-K gate dielectric is important for all high-performance FETs. The transfer characteristics of different dielectric constant of CNTFET is shown in Fig 3. Oxide thickness is kept constant as 1 nm. The output characteristics are simulated for different gate bias varies from 0 V to 1 V keeping V_{DS} is 0.3 V. On current is high for small K dielectric and increases for K value increase.

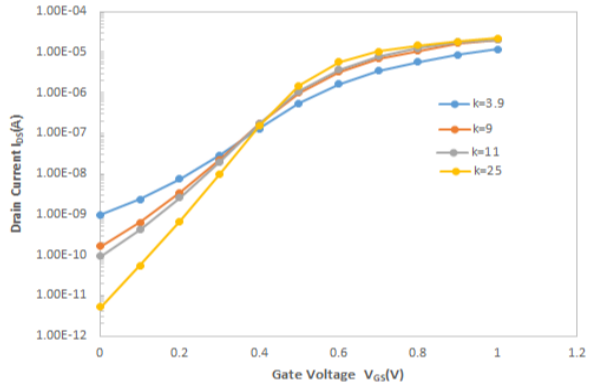

Fig 3-I_{DS}-V_{GS} Characteristics for Different Dielectric constants V_{DS}=0.3V

Table -II Device Performance Parameters

Calculated parameters	**V_{DS} = 0.1 V**	**V_{DS} = 0.5 V**
I_{ON}(A)	7.22E-06	1.32E-05
I_{OFF}(A)	7.52E-10	1.23E-09
I_{ON}/ I_{OFF}	0.96E4	1.07E4
g_m(μS)	17.8	37.9

Table -III Effect of Dielectric constant on I_{ON}/ I_{OFF} at V_{DS}=0.3V

Dielectric Constant(K)	**I_{ON}/I_{OFF}**	**g_m (μS)**
3.9	1.20E+04	30
9	3.27E+05	58
11	2.18E+05	50
25	4.21E+06	48

3. Conclusion

In this paper, different types of dielectric dependent CNTFET is simulated for 5 nm channel length and 0.5 nm diameter using NEGF method. Performance comparison has been done using various parameters Ion/Ioff ratio, transconductance and inverse subthreshold slope. From our simulation it is concluded that for approximately 5 nm device DG-CNTFET offers better performance which is good for low power applications.

References

[1] G Moore, IEDM Tech Digest, (1975) 899.
[2] J. Appenzeller, et al., *IEEE Trans. Electron Devices* 52, 2568 (2005).
[3] A. Javey,et at., Nature 424, 654 (2003).
[4] G. Fiori and G. Iannaccone, NanoTCAD ViDES, 2016
[5] A. Singh, M. Khosla, and B. Raj, J. Nanoelectron. Optoelectron. 11, 388 (2016)