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Thickness Effect of SiGe Layers on SiGe/Si Quantum Well Based Thermistor Performance

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Abstract

This work presents the thickness effect of SiGe layers on $Si_{0.5}Ge_{0.5}$/Si (×3) multi quantum well (MQW) based thermistor performance. As the basic figures of merit for thermistor device, temperature coefficient of resistance (TCR), 1/f noise characteristic and electrical resistance are presented for different thicknesses of SiGe quantum well; 6, 8, 10 nm. Experimental results provide that increasing thickness of SiGe quantum well increases the TCR; however the thermal noise level and the yield over an 8 inch wafer are degraded. Nevertheless, by using an additional carbon delta layer at the interfaces, high overall performance is obtained also with the lowest thickness of SiGe (6 nm) with a lower thermal resistance and with a safe layer quality thus, better process yield on 8 inch wafer.

1. Introduction

Recently, single crystalline SiGe material has attracted an increasing attention as an alternative thermistor material for infrared detection by uncooled microbolometers [1]. The functionality of a thermistor material is based on a change in its electrical resistance due to heating when it is subjected to an infrared radiation. The current commercial technologies for uncooled microbolometers include mainly polycrystalline or amorphous materials as thermistor material, typically vanadium-oxide (VO_x) or amorphous-silicon (a-Si), but their performances are limited in terms of their figures of merit characteristics. On the other hand, single crystalline SiGe/Si multi quantum well (MQW) based structures are reported to be very promising for this application. Recently, a very high temperature sensitivity out of SiGe/Si MQW structure including 50% Ge concentration has been demonstrated [2]. High Ge% content in the SiGe/Si MQW structure results in increasing compressive strain and barrier height thus more amount of confined energy states occurs which increases the number of charge carriers. Therefore, the temperature sensitivity increases by the higher number of charge carriers (holes, in this case). Beside Ge content in the SiGe/Si heterostructure, the number of SiGe quantum well is another factor which could improve the efficiency [3]. However, there is a trade-off relation between increase of the number of SiGe layers and noise as more SiGe/Si interfaces could cause more defects or dislocations in the structure. Additionally, an alternative way to increase the number of charge carrier is increasing the thickness of the SiGe quantum well. However, the thickness of the strained SiGe layers cannot be increased over critical thickness value due to the strain relaxation, which causes defects leading to a limited thermistor performance in the end. Nevertheless, combination of carbon (C) delta layers at the interface of SiGe/Si can also improve both thermal response and noise as it increases the interface quality by preventing of strain relaxation due to elastic deformation [4], thus keeping the Ge% constant in the quantum wells.

In this paper, the thickness effect of SiGe on $Si_{0.5}Ge_{0.5}$/Si (×3) based MQW thermistor performance is presented. The intrinsic thermistor devices with different thicknesses of SiGe quantum wells are compared in terms of their figures of merit characteristics. In addition, an effect of C delta layer incorporation to the interfaces of SiGe/Si MQW structure is presented.

2. Experimental Details

The fabrication details of the intrinsic thermal detector devices are reported previously in [2]. Four different test devices are prepared with a pixel size of 25 µm × 25 µm. Three $Si_{0.5}Ge_{0.5}$/Si (×3) based devices are prepared with 10 nm, 8 nm and 6 nm of SiGe. Another test device is prepared also for 6 nm of SiGe quantum well but with C delta layer incorporation at the SiGe/Si interfaces. The corresponding deposition details for C delta layers are given in [4].

3. Results and Discussions

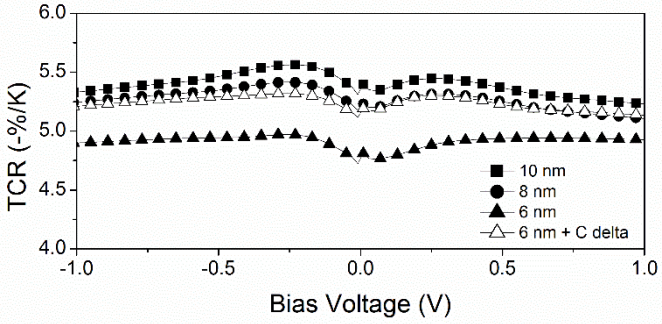

Fig.1 TCR vs. bias voltage measured on SiGe/Si MQW based intrinsic thermistor devices with different SiGe quantum well thickness.

In order to investigate the thickness effect of SiGe quantum wells in terms of TCR value, I-V measurements are performed over a temperature range of 278 K to 323 K on an 8-inch wafer. Fig. 1 shows the extracted TCR values versus bias voltage curves for all the four different thermistor devices. It is clearly seen that the sample with 10 nm of SiGe quantum well has the highest TCR of -5.3 %/K at 0.66 V because of the more charge carriers available for temperature variation sensation. For the cases of 8 nm and 6 nm, TCR values of -5.2 %/K and -4.9 %/K are obtained at the same bias voltage, respectively. Nevertheless, incorporation of C delta layer at the interfaces of the sample with 6 nm SiGe quantum well improves TCR from -4.9 to -5.2 %/K at 0.66 V. The higher TCR value by the additional C layers might be attributed to the suppression of inter-diffusion of Si and Ge at the interface [4], so it prevents decreasing of the maximum Ge concentration in the 6 nm SiGe quantum wells.

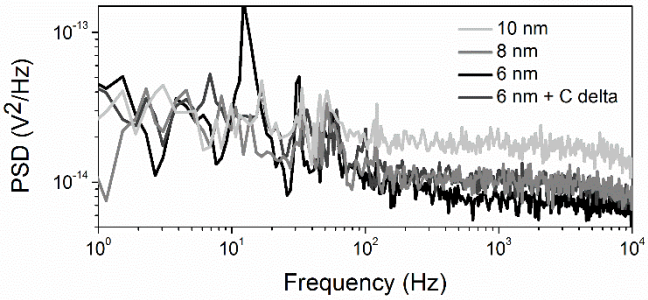

Fig.2 Power spectral density of noise voltage vs. frequency measured at 0.66 V for different intrinsic thermistor devices at room temperature.

Fig. 2 shows noise voltage power spectral densities between 1 and 10^4 Hz obtained on the different intrinsic thermistor devices. All the devices show comparable noise performance with the state of the art thermistors with a $K_{1/f}$ value in the range of e-14 [2]. There is no significant deviation of the performance of the devices from 1/f noise point of view; however, higher thermal noise (Johnson noise) level is observed for the device including 10 nm of SiGe quantum well due to its higher resistance.

Fig. 3 shows the resistance versus bias voltage curves obtained for nine different positions on an 8-inch wafer for the thermistor devices including SiGe quantum wells of 10 nm and 6 nm with additional C delta layers. The higher resistance values is clearly seen for the case of 10 nm. More importantly, variation of the resistance values seem to be more pronounced for the case of 10 nm in comparison with 6 nm and C delta layer case. Table-1 summarizes all the mean resistance values at 0.66 V bias voltage and the standard deviations obtained by nine different measurement positions on 8-inch wafer for all the four different devices. The mean resistance values decreases by the decreasing SiGe quantum well thickness. Although the mean resistance value slightly increases from 172 to 272 kΩ by the additional C delta layers for the case of 6 nm, the lowest standard deviation indicates higher stability against fluctuation of thickness due to strain relaxation over 8-inch wafer scale, which has a significant importance for the yield of the process.

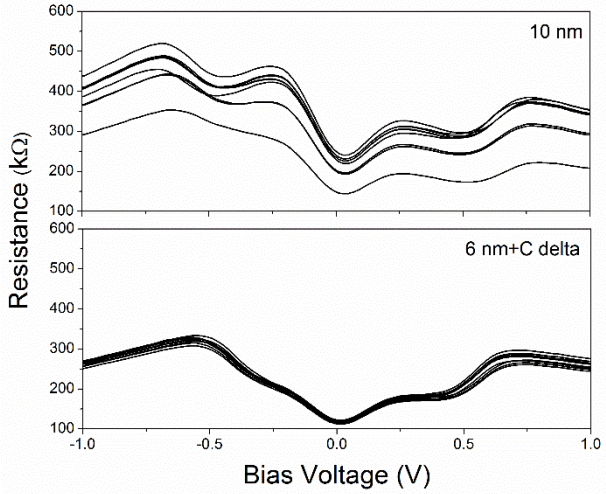

Fig.3 Resistance vs. bias voltage curves measured on nine points over 8-inch wafer for the thermistor devices including SiGe quantum wells of 10 nm and 6 nm with additional C delta layers.

Table I Mean resistance values with the standard deviations at 0.66V

Thermistor	Mean Value at 0.66V	Standard Deviation
10 nm	313 kΩ	±17%
8 nm	211 kΩ	±8.4%
6 nm	172 kΩ	±6.9%
6 nm +C delta	272 kΩ	±5.1%

4. Conclusions

This work presents the thickness effect of SiGe on $Si_{0.5}Ge_{0.5}$/Si (×3) multi quantum well (MQW) based thermistor performance. The thermistor device including 10 nm of SiGe quantum well exhibited a very good performance but with a high resistance variation over 8-inch wafer, thus lower yield. On the other hand, by the incorporation of C delta layer, the device including only 6 nm of quantum well resulted in almost similar figures of merit characteristics as 10 nm case but with a significantly improved resistance variation over the 8-inch wafer. These results are very promising for the use of SiGe/Si MQWs with relatively easy process conditions and beyond state of the art performance figures for microbolometer imaging applications.

References

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