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# Efficient Heat Transfer by Through Silicon Via in 3D Packaging for Practical-scale Quantum Annealing Machine

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**Abstract**

**A Qubit-chip/Interposer/Package substrate (QUIP) structure based on the 3D packaging technology was proposed to realize practical-scale quantum annealing machines. The less effective heat transfer in the stacked structure introduces challenges to the cryogenic environment requirement of qubit chip operation. Therefore, we investigated the thermal conduction of QUIP structure with the finite element method. In order to maintain a cryogenic environment at 20 mK level for qubit chip operation, through silicon via (TSV) structure was proposed to design in the package substrate. The TSVs with larger thermal conductivity than Si provided an efficient heat transfer by connecting directly the generated heat of the active interposer and the heat sink under the package substrate. The maximum temperature of the qubit chip decreased from 139 mK to 16.6 mK when the TSVs were designed in the package substrate. The stable operation temperature for qubit chip can be provided by the design of the TSVs in the QUIP structure.**

## 1. Introduction

Quantum annealing (QA), which was proposed theoretically and examined numerically by Kadowaki and Nishimori, has received considerable interest as a new computing paradigm for solving classical optimization problems by finding the low energy configurations of complicated Ising models [1]. Considering the strictly limited number of available Josephson junctions or superconducting qubits per chip, three-dimensional (3D) integrated technologies provides possibility for realizing a practically large-scale QA machine for solving practical problems. A Qubit-chip/Interposer/Package substrate (QUIP) structure (Fig. 1) was fabricated to realize practical-scale quantum annealing machines in the previous paper [2]. The top qubit chip was mounted on the middle active interposer with superconductor bumps. Five superconducting through silicon vias (TSVs) was set in the active interposer for redundancy design. Considering the thermal contraction during cooling, the same material Si was used for the qubit chip, active interposer, and package substrate. The superconducting material PbIn(9:1) and CuSn(1:9) was set for bump and TSV, respectively. However, thermal challenge of the vertical stacked integrated structure becomes a major concern because the heat spreading in the stack is less effective than non-stacked chips. As the typical qubits are designed to operate at 20 mK temperature level for frequency 5 GHz, the heating of the qubit chip degrades its quantum coherence. Therefore, the thermal conduction analysis was performed with Finite Element Method (FEM) simulation. In order to decrease the temperature of qubit chip, TSV structure was proposed to design in the package substrate.

## 2. Thermal conduction analysis

The thermal conduction analysis was performed with FEM simulation. Owing to the symmetry, a thermal model for a quarterly three chips structure was created and simulated in ANSYS Mechanical Enterprise (version 18.2) to short the computation time (Fig. 2 (a)). The detailed dimensions for the model are given in Table I. The power was estimated as 1 nW for readout, and 1 pW for Digital-to-Analog Converter (DAC) writing. As a maximum 32 nW was set for 20.48 $mm^2$ area, heat flux boundary condition of 1.56nW/$mm^2$ was set on the top face of the active interposer. An ideal heat sink held at 10 mK was assumed at the bottom of the package substrate. To the best of authors knowledge, the measured value of the thermal conductivity at 10 mK for material Si, PbIn(9:1), and CuSn(1:9) was not available yet. The extrapolation method was used to achieve the thermal conductivity at 10 mK. The value of Sn was used for CuSn(1:9). The value of the thermal conductivity for each material and the corresponding reference was listed in Table II.

The simulation results showed the temperature distribution of QUIP structure (Fig. 2 (b)). The heat generated by the active interposer can't transfer efficiently to the heat sink. The quantum coherence of the qubit chip degrades as the maximum temperature 139 mK is 6 times larger than the operation temperature 20 mK. In order to decrease the maximum temperature for qubit chip, the number of TSVs and bumps was increased from 5 to 49 with a 7x7 layout shown in Fig. 3 (a). Although the maximum temperature of qubit chip decreased to 35 mK (Fig. 3 (b)), it is still higher than the normal operation temperature. We proposed an idea to optimize the heat transfer to heat sink. The TSVs with larger thermal conductivity were designed in the Si substrate to connect thoroughly the generated heat and the heat sink (Fig. 4). Figure 5 showed the quarterly FEM model with five TSVs in the active interposer and the substrate, and its temperature distribution results. As the TSV connected thoroughly the generated heat from active interposer and the heat sink under package substrate, the heat was transfer efficiently to the heat sink. The maximum temperature of qubit chip decreased from 139 mK

to 16.6 mK, which is under the operation temperature 20 mK.

## 3. Conclusions

A QUIP structure was fabricated to stack vertically the qubit chip, active interposer, and substrate to realize practical-scale quantum annealing machines. Stacking three chips vertically caused the heat spreading less effective than non-stacked chips. Therefore, the thermal conduction was investigated with FEM simulation. In order to fulfill the requirement of the cryogenic environment for qubit chip operation, TSV structure was proposed to design in the package substrate. As the TSVs with larger thermal conductivity than Si connected thoroughly the generated heat from active interposer and the heat sink under package substrate, the heat was transfer efficiently to the heat sink. The maximum temperature decreased to 12% with a value under the operation temperature 20 mK, when TSVs was designed in the package substrate.

The stable operation temperature can be provided by the TSVs in the QUIP structure. The temperature measurements will be performed on the sample with TSV in the future.


## Acknowledgements

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## References


[1] T. Kadowaki and H. Nishimori, Phys. Rev. E. **58** (1998) 5355.

[2] M. Maezawa, et al. J. Phys. Soc. Jpn. **88** (2019) 061012.

[3] http://www.efunda.com/materials/elements/TC_Table.cfm?Element_ID=Si

[4] A.K. Gupta and S. Wolf, PRB **6** (1972) 2595.

[5] https://www.efunda.com/materials/elements/TC_Table.cfm?Element_ID=Sn


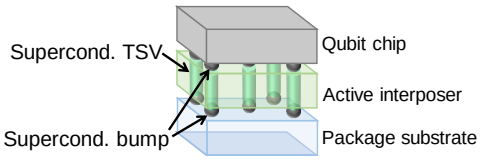


Fig. 1 Schematic of the Qubit-chip/Interposer/Package substrate (QUIP) structure to realize practical-scale quantum annealing machines. The top qubit chip was mounted on the middle active interposer with superconductor bumps. The superconducting through silicon vias (TSVs) was set in the active interposer

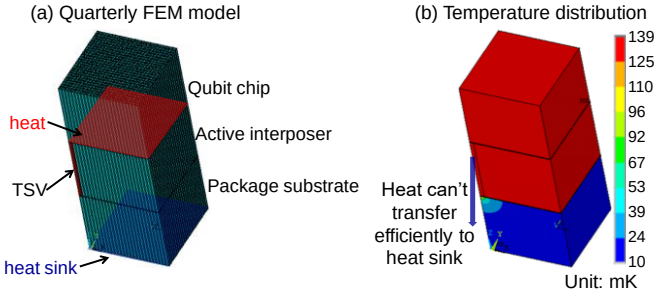


Fig. 2 (a) Quarterly FEM model, (b) Temperature distribution of QUIP structure. The heat generated by the active interposer can't transfer efficiently to the heat sink. The maximum temperature 139 mK, which is 6 times larger than the normal operation temperature of 20 mK. The heating of the qubit chip degrades its quantum coherence.

Table I Modeling dimensions

| | Length/width (μm) | Height (μm) |
|---|---|---|
| Each chip (Qubit chip; Active interposer; package substrate) | 1000 | 400 |
| Bump | Diameter 10 | 4 |
| TSV | Diameter 50 | 400 |

Table II Material Properties

| Material | Thermal conductivity (W/mK)@10 mK |
|---|---|
| Si [3] | 6.22e-05 |
| Bump PbIn(9:1) [4] | 3.28e-01 |
| TSV CuSn(1:9) [5] | 3.21e-01 |

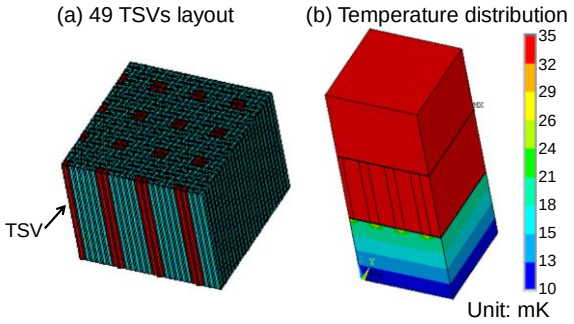


Fig. 3 (a) 49 TSVs layout in the active interposer, (b) Temperature distribution of the QUIP structure with 49 TSVs. The maximum temperature of 35 mK for qubit chip is higher than the normal operation temperature of 20 mK.

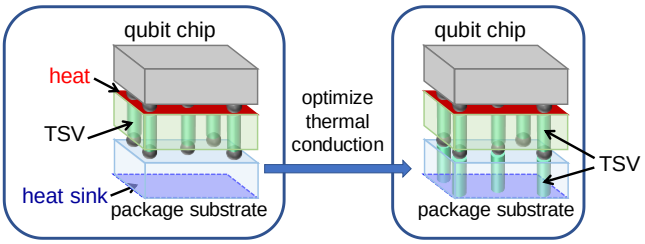


Fig. 4 In order to optimize the heat transfer to heat sink, TSV structure was proposed to design in the package substrate to connect thoroughly the generated heat and the heat sink.

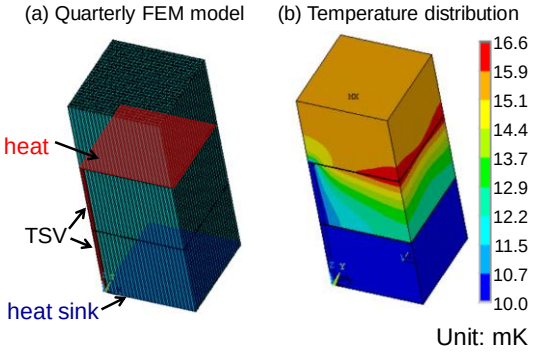


Fig. 5 (a) Quarterly FEM model, (b) Temperature distribution of the QUIP structure with TSVs in the substrate. The TSVs with larger thermal conductivity than Si connected the generated heat from the active interposer thoroughly to the heat sink under the substrate to provide an efficient heat transfer. The maximum temperature decreased from 139 mK to 16.6 mK, which is low enough to provide normal operation for qubit chip.