Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp1045-1046

Gain control circuit for audio mixer utilizing CAAC-IGZO FETs

Kiyotaka Kimura, Takeya Hirose, Yoshinori Ando, Hidetomo Kobayashi,
Takayuki Ikeda and Shunpei Yamazaki[1]

Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa, 243-0036, Japan
Phone: +81-46-248-1131, Fax: +81-46-270-3751, E-mail: kk1308@sel.co.jp

Abstract

An audio mixer circuit having a sample and hold (S/H) circuit including a c-axis aligned In-Ga-Zn oxide (CAAC-IGZO) FET amplifies an input signal by multiplying the input signal with an analog voltage in Gilbert cells, where the analog voltage is stored in the S/H circuit. This method controls gain of multiple channels with one D/A converter, thus shrinking the circuit. A Gilbert cell with the S/H circuit was prototyped and measured, and the precision of the Gilbert cell's output waveforms was stable regardless of whether or not the S/H circuit held data.

1. Introduction

Audio codecs are used in a variety of applications for analog-to-digital encoding and digital-to-analog decoding. One channel requires one separate gain control circuit to be implemented in the audio codec's mixers, which means that using a larger number of channels result in larger circuit area and power consumption. This work aims to solve this issue by using one D/A converter to control the gain of all channels in a mixer, thereby simplifying the circuit.

2. Circuit Design

First, we describe the configuration of this work's gain control circuit. Fig. 1 is a block diagram of the case when there are four channels. The gain control circuit is composed of Gilbert cells (GIL), a D/A converter (DAC), and a logic circuit (Logic), and one Gilbert cell is provided for one channel.

The audio signal input to each channel is amplified through the analog voltage multiplication in the Gilbert cell and then output. Input signals Vinp[3:0] and Vinn[3:0] are differential signals. The gain is determined by the logic circuit and is output as digital data. The digital data signal is converted to an analog voltage in the D/A converter, and is output to the Gilbert cell. By implementing analog data retention function in the Gilbert cell using sample and hold (S/H) circuits, the voltage output from the D/A converter can be retained in the Gilbert cell. The D/A converter sequentially writes different analog voltage to Gilbert cells each corresponding to a channel. Therefore, using this configuration, the gain of multiple channels is controlled using one D/A converter.

Fig. 2 is a circuit diagram of a Gilbert cell. Vinp and Vinn are input signals, and Vwp and Vwn are analog voltages that determine the input gain. This Gilbert cell has an S/H circuit composed of a capacitor and a CAAC-IGZO FET (functioning as an analog switch) in addition to a

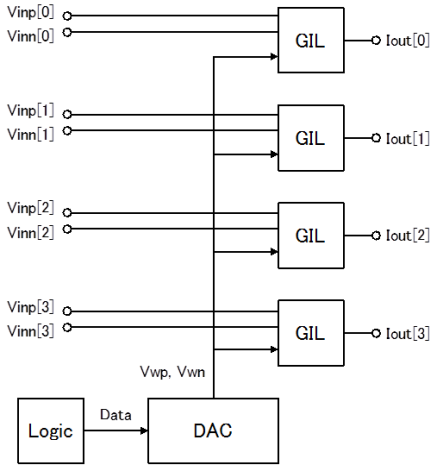

Fig. 1 Block diagram of this work's gain control circuit in the audio mixer.

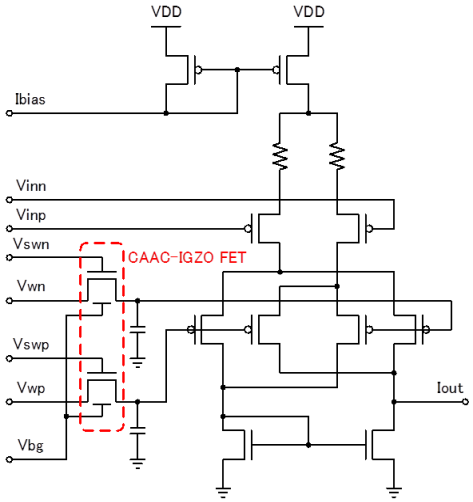

Fig. 2 Circuit diagram of the Gilbert cell with sample and hold circuit having CAAC-IGZO FETs.

conventional Gilbert cell configured with Si FETs, enabling this Gilbert cell to retain Vwp and Vwn values. The CAAC-IGZO FET has an extremely low off-state leakage current on the order of yoctoamperes (yocto- is a prefix denoting a factor of 10^{-24}) which enables a long-term charge retention. The data hold performance of the S/H circuit can be adjusted with the voltage applied to the CAAC-IGZO FET's back gate (Vbg).

3. Prototyping and implementation of the Gilbert cell

A Gilbert cell having the S/H circuit with CAAC-IGZO FETs was prototyped using a process technology that

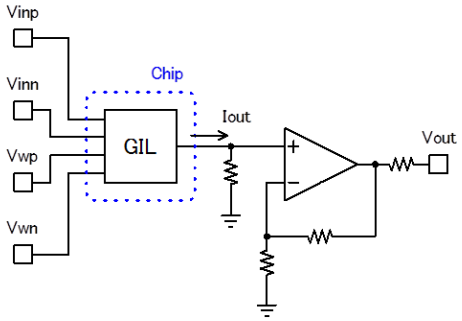

Fig. 3 Implementation of the Gilbert cell in this prototype.

combines 0.11 μm Si CMOS and 60 nm CAAC-IGZO technologies.

The chip was implemented via wire-bonding, as illustrated in Fig. 3. The input signals Vinp and Vinn, and the analog voltages Vwp and Vwn that determine the gain are supplied from external sources. The output current Iout is converted into voltage through a resistor, and an amplifier amplifies the voltage to output Vout.

Power supply voltage of this circuit is 3.3 V, and the peak-to-peak value in each of Vinp, Vinn, Vwp and Vwn is 0.4 V to retain the output linearity of the Gilbert cell.

4. THD + N performance

When the analog voltage is held by turning off the CAAC-IGZO FET, voltages Vwp and Vwn become floating. There is a concern that operating the Gilbert cell in this condition may change the Vwp and Vwn levels. To verify this, we evaluated the THD + N performance of the Gilbert cell. For this measurement, we input 1 kHz sine waves into Vinp and Vinn and fixed voltages to Vwp and Vwn, and measured the Vout waveforms for two cases: the first case has the CAAC-IGZO FET turned on, and the second case has the CAAC-IGZO FET turned off and Vwn held in the capacitor. Fig. 4 is the FFT spectra of Vout. THD + N performance was 12% when the CAAC-IGZO FET was turned on, and 14% when the voltage Vwn was held with the CAAC-IGZO FET turned off. Thus, the Gilbert cell exhibited comparable THD + N performance in both cases. Therefore, even when the S/H circuit holds the voltage, the Vwn is kept at a constant level.

5. Analog voltage hold time

The Vwp and Vwn hold time of the S/H circuit having CAAC-IGZO FETs was measured. For this measurement, we input 1 kHz sine waves into Vinp and Vinn and fixed voltages to Vwp and Vwn. We turned off the CAAC-IGZO FET in the S/H circuit so that Vwn is held in the hold capacitor. Considering the Vout's peak-to-peak value at this time as the initial value, we measured its change over time. The measurement was conducted for different back gate voltage Vbg of the CAAC-IGZO FET: 4 V, 4.5 V, 5 V, and 5.5 V. Fig. 5 illustrates the relationship between the time and ΔVpp, which is the amount of decay in Vout's peak-to-peak value from the initial value. Smaller Vbg resulted in smaller ΔVpp change, and when Vbg = 4 V, the ΔVpp after 0.2 s was 0.012 V. Reducing the Vbg further can be expected to yield longer data hold time.

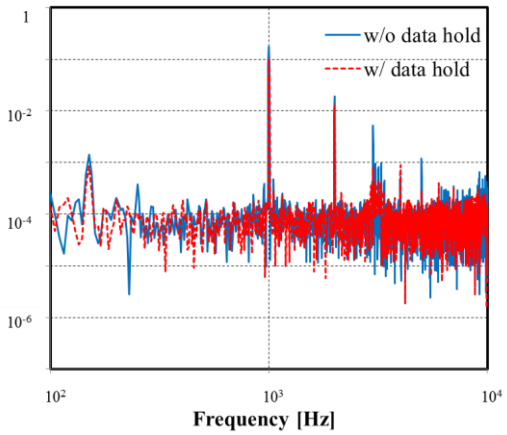

Fig. 4 FFT spectra of output waveforms.

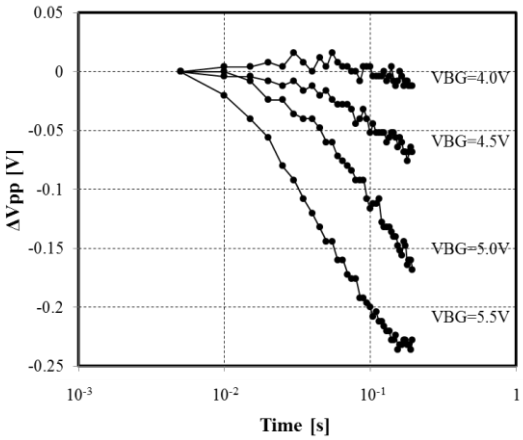

Fig. 5 Time-dependent change of the peak-to-peak values in the output waveform.

6. Conclusion

We prototyped a circuit in which Gilbert cells amplify an input signal by analog voltage multiplication, and a sample and hold (S/H) circuit having *c*-axis aligned In-Ga-Zn oxide (CAAC-IGZO) FETs retains the analog voltage used in the multiplication. The purpose of this circuit is to control the gain of all channels in an audio mixer using one D/A converter. An analog voltage could be stored with little change over time using the S/H circuit, even when the Gilbert cell is operating.

References

[1] S. Yamazaki *et al, J. Soc. Info. Disp.* 22, 55-67 (2014).
[2] S. Yamazaki *et al, J Solid State Sci. Tech.* 3 (9) *Q*3012-*Q*3022 (2014).
[3] K. Kato *et al, Jpn. J. Appl. Phys*. 51, 021201 (2012).
[4] Y. Yakubo *et al, presented at E*-7-1 *Int. Conf. Solid State Dev. Mat.* (2014), *p.*648.
[5] Y. Kobayashi *et al, Jpn. J. Appl. Phys.* 53, 04*EF*03 (2014).