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Sub-35 nm SiC Strained nMOSFETs with Super-400 GHz f_T for mm-wave CMOS Design

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Abstract

Silicon-Carbon (SiC) strained nMOSFETs with sub-35 nm gate length in 40 nm CMOS technology can realize superior cut-off frequency (f_T) up to 405 GHz, attributed to more than 20% enhancement of the effective mobility (μ_{eff}) and transconductance. This super-400 GHz f_T makes SiC strained nMOS a competitive nano Si device solution aimed at mm-wave CMOS circuits design.

I. Introduction

Nanoscale CMOS devices with mobility enhancement from uniaxial strain have been proven successful for driving high speed logic circuits and superior high frequency performance like f_T and f_{MAX} for RF and mm-wave circuits design [1]-[3]. For nMOSFETs in favor of high frequency design, tensile strain is the right choice and contact etching stop layer (CESL) by a nitride liner has been most widely used to create tensile $\sigma_{//}$ for electron mobility enhancement since 90 nm technology node and scaling to 65nm node [1]. Unfortunately, the tensile $\sigma_{//}$ from CESL becomes less effective when further scaling to beyond 65 nm node, due to the stress degradation caused by the aggressive shrinkage of pitch rule and nitride liner thickness. SiC strain embedded in the source/drain region appears as a new solution for achieving sufficient tensile $\sigma_{//}$ for nMOSFETs at 45 nm node and beyond [4]-[5]. In this paper, SiC strained nMOSFETs with sub-35nm gate length fabricated in 40 nm CMOS technology can achieve superior f_T up to 405 GHz, which is around 25% enhancement over the control nMOS without strain engineering.

II. I-V and High Frequency Characterization for sub-40nm nMOS– μ_{eff} enhancement in SiC strain nMOS

First, as shown in Fig. 1(a), SiC strained nMOSFETs were implemented by Silicon-Carbon solid phase epitaxy (SPE) in S/D extension (SDE) region for achieving enhanced tensile $\sigma_{//}$ [5]. At the same time, control and SiC strained nMOSFETs were fabricated in 40 nm high performance CMOS technology with ultra-thin gate oxide of 1.2 nm (T_{ox}=12Å) and drawn gate length at min. rule, L=40nm. Fig. 1(b) illustrates multi-finger (MF) MOSFET layout with three variations of W_F and N_F at fixed $W_{tot}=W_F\times N_F$=32 μm, namely W2N16, W05N64, and W025N128 to verify the optimized layout for the maximum f_T. S-parameters were measured by vector network analyzer Keysight E8364B. Open and short deembedding have been carried out to the bottom metal, i.e. M1 for achieving intrinsic Y-, Z-, and H-parameters and a comparison of intrinsic f_T between the control and SiC strained nMOSFETs. Fig. 2(a) and (b) present the intrinsic gate capacitances $C_{gg}=\mathrm{Im}(Y_{11})/\omega$ achieved from the control and SiC strained nMOSFETs with 3 sets of MF layouts, i.e. W2N16, W05N64, and W025N128. The comparison of C_{gg} indicates similar frequency and layout dependence, such as an obvious increase of C_{gg} at smaller W_F and larger N_F even at the same W_{tot}.

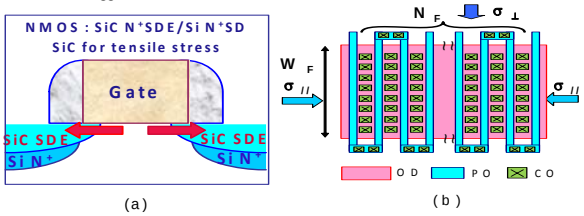

Fig. 1 (a) SiC strained nMOS with tensile $\sigma_{//}$ created by SiC SPE in SDE (b) multi-finger MOSFETs with various W_F and N_F at $W_{tot}=W_F\times N_F$ =32 μm, W2N16, W05N64, and W025N128.

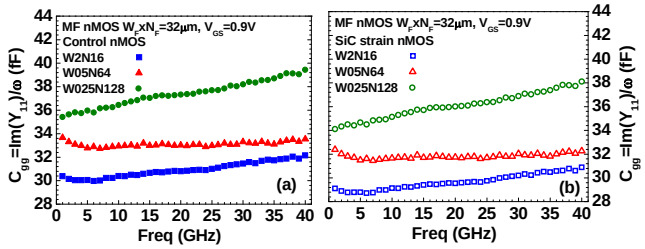

Fig. 2 Intrinsic gate capacitance C_{gg} =Im(Y_{11})/ω (V_{GS}=0.9V, V_{DS}=0.05V) achieved after openM1 and shortM1 deemebdding (a) control nMOS (b) SiC strained multi-finger nMOS, W2N16, W05N64, W025N128.

3-D interconnect capacitance simulation by Raphael can be done to investigate the layout dependence of C_{gg} in MF MOSFETs. As shown in Fig. 3, the gate sidewall and finger-end fringing capacitances, namely C_{of} and $C_{f(poly\text{-}end)}$ appear as the key factors responsible for the increase of C_{gg} in case of larger N_F and smaller W_F. The C_{gg} vs. N_F associated with control and SiC strained nMOS, shown in Fig. 4(a) and (b) demonstrate a linear function, which can be predicted by our derived analytical model given by (1) with the slope α and intercept β given by (2) and (3) [6]-[7]. Through an iteration flow, the basic device parameters can be precisely extracted for control/SiC strained nMOSFETs, given as L_g=35.05nm/32.85nm, ΔW=32.16nm, and $T_{ox(inv)}$=1.95nm, which are necessary for accurate extraction of μ_{eff} from linear I-V characteristics, according to (4)~(5).

$$C_{gg} = \alpha N_F + \beta \tag{1}$$

$$\alpha = C_{f(poly-end)} + \Delta W\left(C_{ox(inv)}L_g + C_{of}\right) \tag{2}$$

$$\beta = \left(C_{ox(inv)}L_g + C_{of}\right)W_{tot},\ W_{tot} = W_F \times N_F \tag{3}$$

$$I_{DS} = \frac{W_{eff}}{L_g}C_{ox(inv)}\mu_{eff}\left(V_{GS} - V_T - \eta V_{DS}\right)V_{DS},\ 0 < \eta \le \frac{1}{2} \tag{4}$$

$$\mu_{eff} = \frac{L_g}{W_{eff}C_{ox(inv)}} \cdot \frac{I_{DS}}{\left(V_{GS} - V_T - \eta V_{DS}\right)V_{DS}},\ W_{eff} = \left(W_F + \Delta W\right)\cdot N_F \tag{5}$$

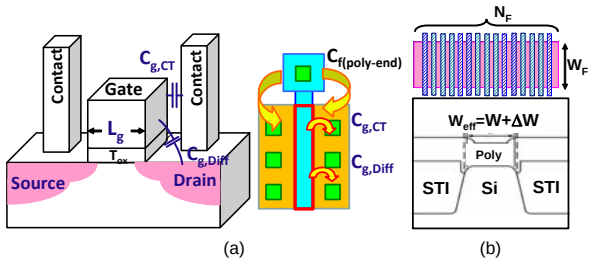

Fig.3 (a) Schematics of MOSFET with L_g, $T_{ox(inv)}$, gate sidewall and finger-end fringing capacitance C_{of}=$C_{g,Diff}$ +$C_{g,CT}$ and $C_{f(poly\text{-}end)}$ (b) multi-finger MOSFET cross section showing ΔW due to STI top corner rounding and increase of W_{eff}.

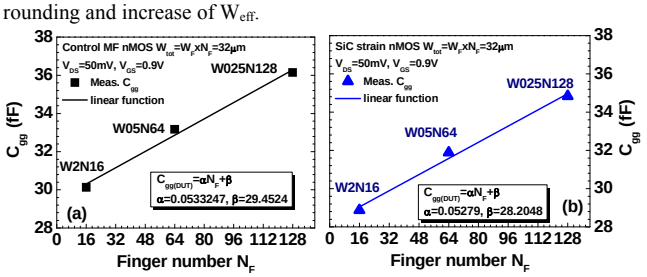

Fig.4 $C_{gg(}$ vs. N_F of multi-finger nMOSFETs with various W_F and N_F at fixed W_{tot}=32 μm – a linear function of N_F with the slope α and intercept β (a) control nMOS (b) SiC strained nMOS in linear region at V_{DS}=50mV.

Fig. 5 (a) and (b) present very promising result that SiC strained nMOS can deliver 22.5% and 26% increase at I_{DS} and g_m than control nMOS with the same layout, similar $T_{ox(inv)}$ and ΔW, but a minor difference at L_g (35.05nm/32.85nm). In the following, μ_{eff} can be extracted from the linear I-V model, given by (4) and (5) in which L_g, $C_{ox(inv)}$, and ΔW have been known. As shown in Fig. 6, the SiC strained nMOS can successfully realize 20~27% higher μ_{eff} through V_{GT} and near 23% enhancement of the peak μ_{eff}, compared to the control nMOS,

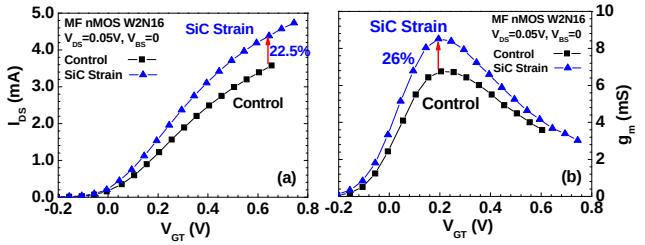

Fig. 5 (a) I_{DS} vs.V_{GT} (b) g_m vs.V_{GT} at V_{DS} = 0.05V measured from control and SiC strained MF nMOS with W_F=2μm,N_F=16 (W2N16).

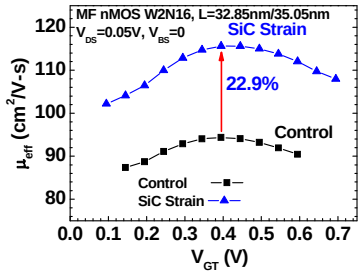

Fig.6 Comparison of μ_{eff} vs.V_{GT} (V_{DS} =0.05V) extracted from SiC strained nMOS (L_g=32.85nm) and control nMOS (L_g=35.05nm) MF layout W2N16

III. High frequency performance enhancement in high mobility SiC strained nMOS – Super-400GHz f_T

The prominent enhancement of μ_{eff} and g_m realized by SiC strained nMOSFET suggests achievable improvement on high frequency performance like f_T. First, g_m, C_{gg}, and C_{gd} identified as three key device parameters responsible for f_T, can be determined by the intrinsic Y-parameters, according to (6) ~ (8) and analytical model for f_T given by (9). Note that f_T calculated by (9) as a function of g_m, C_{gg}, and C_{gd}, denoted as f_T@model can facilitate understanding of the multi-finger layout dependence and optimization principle for the maximum f_T.

$$g_m = \mathrm{Re}(Y_{21}) \tag{6}$$

$$C_{gg} = \frac{\mathrm{Im}(Y_{11})}{\omega} \tag{7}$$

$$C_{gd} = \frac{-\mathrm{Im}(Y_{12})}{\omega} \tag{8}$$

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \tag{9}$$

Fig. 7(a) ~ (b) present the results for control nMOS (solid symbols) and SiC strained nMOS (empty symbols) with 3 sets of MF layouts, i.e. W2N16, W05N64, and W025N128. Both types of nMOS indicate similar layout dependence, such as minor difference at g_m among 3 MF layouts but significant increase of C_{gg} at larger N_F and smaller W_F denoted as $(C_{(poly\text{-}end)}+(C_{ox(inv)}L_g+C_{of})\Delta W)N_F$, i.e. αN_F given by (1) ~(2). It can be understood from f_T@model given by (9) that similar g_m and larger C_{gg} will lead to f_T degradation, i.e. the larger N_F the lower f_T. Thus the maximum f_T can be achieved by W2N16 with the smallest C_{gg}, such as peak f_T up to 302 GHz for control nMOS and even much higher to 405 GHz for SiC strained nMOS. A comprehensive comparison indicates that SiC strained nMOS can realize 24 ~ 26% enhancement of f_T than control nMOS due to 15~16% higher g_m in saturation region partly from μ_{eff} enhancement and around 6% smaller C_{gg}, primarily due to shorter L_g. Moreover, f_T can be determined by unit current gain, i.e. f_T@$|H_{21}|$=1 and the results shown in Fig.8(a) and (b) demonstrate a good agreement between the f_T@$|H_{21}|$=1 (symbols) and f_T@model (lines) for control and SiC strained nMOS. It proves that the model given by (9) can accurately predict the f_T for control and SiC strained nMOS, and more importantly the layout dependent effects for high frequency performance optimization. The super-400 GHz f_T makes SiC strained nMOS an attractive and competitive solution for mm-wave CMOS circuits design.

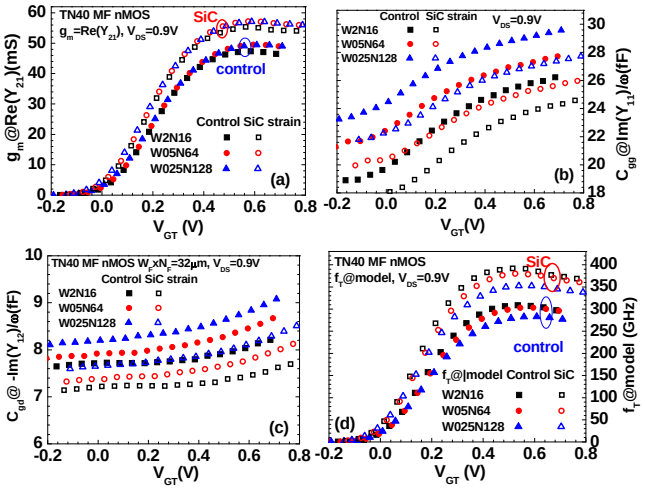

Fig. 7 Comparison of control and SiC strained nMOSFETs with various N_F and W_F at $N_F \times W_F$ =32 μm (a) g_m@Y=Re(Y_{21}) (b) C_{gg}=Im(Y_{11})/ω (c) C_{gd}=-Im(Y_{12})/ω (d) f_T@|model at V_{DS}=0.9V and various V_{GT}

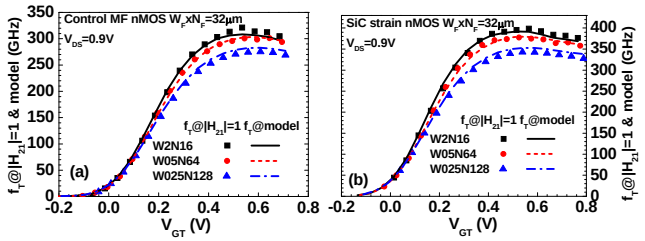

Fig. 8 Comparison of f_T@$|H_{21}|$=1 (symbols) and f_T@model (lines) versus V_{GT} at V_{DS}=0.9V (a) control nMOS (b) SiC strained nMOS with MF layouts W2N16, W05N64, and W025N128

IV. Conclusion

The SiC strained nMOS can successfully realize 24~26% higher f_T and the peak f_T up to 405 GHz at sub-35 nm gate length. The analytical model derived for f_T can accurately predict f_T@$|H_{21}|$=1 versus V_{GT} and more importantly MF layout optimization for achieving the maximum f_T. The SiC strained nMOSFETs with super-400 GHz f_T at optimized MF layout appear as a very competitive solution for high mobility devices aimed at mm-wave CMOS circuits design.

References

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