Evaluation of bending stress in Au-wiring formed over FHE by micro-XRD

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Abstract

Au redistribution layer was fabricated over heterogeneously integrated advanced flexible hybrid electronics (FHE) substrates formed via die-first approach based on Fan-Out Wafer-Level Packaging (FOWLP). As formed Au metal wirings were meticulously studied for the locally induced mechanical stress upon bending (bending radius, BR 20 mm) by micro-X-ray diffraction (µ-XRD) using synchrotron radiation. µ-XRD results revealed that upon bending the FHE substrate to the BR of 20 mm, has exerted a mechanical stress to the magnitude of 250~300 MPa in the 100 µm-width, 10 mm-long and 500 nm-thick Au metal wiring. The observed actual stress values from µ-XRD data for the Au metal wirings were nearly 2x larger than the stress value of 138 MPa obtained by simulation studies.

Introduction

Typical flexible hybrid electronics (FHE) fabrication involves the combination of processes such as the hetero integration of ultra-thin IC/LSI dielets/chiplets on to the flexible substrate (to make them bendable to follow curved profiles of the mounting surface) and the printable wiring technologies over the flexible substrate. One of the most important criteria for the embedded dielets/chiplets of the flexible substrate is the maximum flexibility (or the smaller bending radius) that they can withstand, since the mounted dielets/chiplets (containing functional devices) on flexible substrate follow curved profiles of the mounting corrugated surface. To achieve the smaller bending radius with maximum flexibility of the functional LSI dielets/chiplets, the thickness of the die/chip has been brought down to less than 50 µm. Since these ultrathin dies embedded/mounted on flexible substrate are very sensitive to external pressures, that may affect the performance and property deviation of devices at smaller the bending radius environment. Our previous investigations revealed that not only the most critical parameter, the retention time, for the 50 µm-thick stacked Dynamic Random Access Memory (DRAM) with planar capacitors was worst affected [1], but also the very inherent properties of bulk Si, the hardness and the modulus values were altered for the die thickness going from 50 μ m to less than 10 μ m [2-4].

Thus, it is worth to investigate the effect of bending radius (BR) of FHE on the Au metal wire and the ultrathin Si chips. In this work we have investigated the remnant mechanical stress in the Au metal wires on FHE by μ -XRD using sync. radiation and compared the results with the simulation data.

Experiment

As shown in schematic process flow (fig. 1), either 100 µm-thick Si chiplets (1 mm x 1 mm) or 200-µmthick LSI chips (2.5 mm x 2.5 mm) with photodiode and LED driver circuits are embedded into PDMS (biomedical grade) using double Si carrier wafers. Before the PDMS charging, the chiplets were face-down placed on the 1st carrier wafer. Then the chiplets-onwafer were covered by monomers of PDMS, followed by degassing in vacuum and subsequently wafer level compression molding with the 2nd carrier. After the debonding of 1st carrier, chiplets were planarized without any mechanical processes. Prior to the following metallization processes, a single stress-bufferlayer SBL was coated on the PDMS/chiplets. By using standard photolithography with metal sputtering/wet etching, 200-nm-thick Au wirings were formed on the SBL(s) at the wafer-level. Finally, the integrated FHE were debonded from the 2nd carrier to obtain freestanding FHE systems.

Results and Discussion

Optical microscopic (OM) images in fig.2 are obtained for the 200 nm-thick Au wiring formed over (a) organic substrate and (b) the embedded Si chips, and (d)-(e) are their respective magnified OM images. Using our die-first approach, from 100 μ m-width to as narrow as 10 μ m-width Au wiring over 10 mm length were formed successfully as shown in fig. 2 c.

In order to estimate the expected mechanical stress values in Au wiring on FHE substrate induced by bending prior to the µ-XRD experiments, we did carryout the simulation studies using ANSYS for similar environment and results are depicted in fig. 3. The simulations were carried out for the concave bending with the BR ranging from 5 mm to 20 mm as shown in fig. 3(a). The Poisson's ratio of 0.49 for PDMS, 0.42 for Au, and 0.22 for Si, their respective CTE (ppm/K) of 300, 14.2 and 3, and the Young's modulus (GPa) of 5e-4, 79 and 190 were used in the simulation studies. The obtained von Mises stress distribution in the FHE substrate is depicted in fig. 3(b). It is inferred that the stress in the Au wiring accumulates near the ridges, and the maximum stress value is around ~137 MPa. The stress magnitude in the Au wire tends to decrease, as one moves away from the chiplets. On the other, the 100 µmthick Si chiplets does not experience any local mechanical stress upon bending.

Having estimated the amount of bending stress in Au wirings, we did collect the micro-diffraction data of Au (111) peak on the FHE substrates at the BR of 20 mm and the obtained stress values are shown in fig. 4. The stress values at 15 different points with 10 μ minterval in both X and Y direction fluctuate between 250 MPa and 310 MPa. The measured stress values are nearly 2x larger than the stress value estimated by simulation. One plausible reason is the grain size of Au and surface roughness of the polymer surface over which the Au wirings are formed. In simulation these two parameters are not considered, but their existence is real as can be seen from the optical image of Au-RDL in fig. 4(b). We did not either observe any trend in the change of measured stress values, as one going from the center to the periphery of the Au wire on the



Fig. 1 Schematic process flow diagram for the formation of FHE system







Fig. 4a Residual remnant stress present in the 100 μm -width Au metal wire when subjected to bending up to the BR of 20 mm.

flexible part of the FHE. It may be necessary to either improve the surface flatness of the organic film prior to the Au deposition or else to modify the SBL itself to bring down the bending stress.

Conclusions

 μ -XRD analysis on FHE with Au wiring formed by die-first approach revealed that Au wiring over organic part experiences bending stress to the maximum of ~300 MPa under the 20 mm BR configuration. While the simulation results showed that the bending stress in Au wires over organic part diminishes as one move farther off from the chiplet ridges, and near-zero stress value over the chiplets. Thus, a 100 μ m-thick chiplets are good enough to fabricate robust FHE.

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References: [1] K.W. Lee *et al*, IEEE TED, 61 (2014) 379; [2] M. Murugesan *et al*, Proc. ASMC2013, p.66; [3] M. Murugesan *et al*, IEEE TSM, 27(2014) 341; [4] M. Murugesan *et al*, IEEE TED, 61 (2014) 540.



Fig. 3a Ansys simulation results for flexible substrate bending



Fig. 3b Stress distribution in Au wires on the flexible substrate



Fig. 4b OM image of 100 μm -width Au metal wire spreads across the FHE substrate