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Novel Stacking Technologies for The Stacked CMOS Image Sensors

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***Abstract*—In this paper our 3D chip stacking technologies for CMOS image sensors (CISs) are introduced. We have developed Through-Silicon-Via (TSV) technology and Cu-Cu direct bonding technology for stacked BI-CIS. Our 3D chip stacking technologies have successfully realized the multifunctional, high-performance and highly productive CIS devices. Such innovative technologies are expected to evolve not only the CIS devices but also the general 3D stacked semiconductor devices.**

I. INTRODUCTION

We are consciously and unconsciously benefiting from the spread of the Internet of Things (IoT). With this spread comes the strong demand for various semiconductors, especially small, multifunctional, high-performance LSIs. A promising solution is a system in package (SiP) such as a multi-chip 2D package or a 3D stack package. 3D chip stacking technology in particular can easily implement different function chips in a small system. We have contributed to the development of multifunctional and high-performance CMOS image sensors (CISs) with various 3D chip stacking approaches for many years. This paper introduces our innovative 3D chip stacking technologies that have achieved our advanced CIS devices.

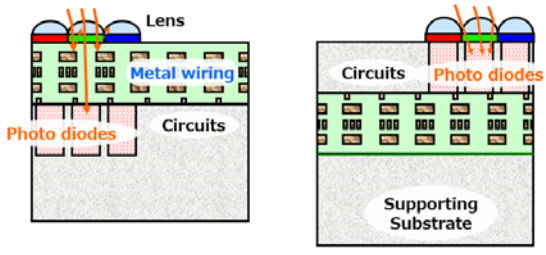

Fig. 1. Schematic diagrams of FI-CIS (left) and BI-CIS (right)

II. STACKED BI-CIS

We developed a CIS device with metal wiring under the photo-diode, which is called a back-illuminated CIS (BI-CIS) [1]. As shown in Figure1, BI-CIS can effectively collect light into photo diodes without reflection of metal wiring that degrade the sensitivity in conventional front-illuminated CIS (FI-CIS). We confirmed that the device offers higher sensitivity and better performance in optical shading without any degradation in the device performance.

In addition to the image quality, speed, and pixel counts that conventional image sensors require, there was high demand for new functions that can respond to various photo-taking scenes. We have developed a stacked BI-CIS, composed of conventional back-illuminated image sensor technology and 65nm standard logic technology [2-4]. As shown in Figure 2, the stacked BI-CIS uses a logic process substrate in place of a blank carrier wafer of the conventional BI-CIS, and thus forms advanced logic circuits using an exclusive logic process technology that is independent of the CIS process.

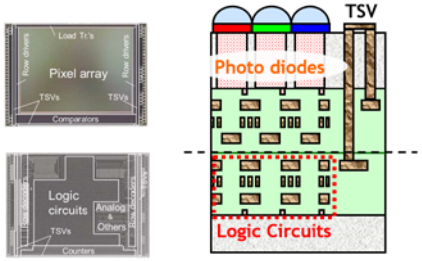

Fig. 2. Schematic diagrams of Stacked BI-CIS

In the early type of stacked BI-CIS the Through-Silicon-Via (TSV) technology was used to electrically connect upper CIS chip and lower logic chip. Figure 3 shows the resistance distributions of the TSV chain module. The number of connections is 15K. The tight distribution shows good electrical connectivity.

Fig. 3. Cumulative plot of contact resistance of each TSV

III. CU-CU DIRECT BONDING

To fabricate high-performance and highly productive stacked BI-CIS, we have developed a unique 3D stacking technology: Cu-Cu direct bonding as illustrated in Figure 4. Firstly, we have released the stacked BI-CIS

with 6 µm-pitch and 20K Cu-Cu connections [5]. As shown in Figure 5 (left), the Cu-Cu connections were located at peripheral area of pixel arrays and logic circuits in this device. The Cu-Cu connections have a lot of advantages from view point of layout flexibility compared with the conventional chip stacking technologies such as TSV. We can place the Cu-Cu connections not only at the peripheral area but also at the central area of upper/lower chip. By making use of the circuit design flexibility, we have recently developed a new BI-CIS device [6]. In that device, each pixel at upper chip was directly connected to the A/D converter circuit at lower chip thorough the 6.9 µm-pitch and 3M Cu-Cu connections that were placed at the whole area of upper/lower chip as illustrated in Figure 5 (right).

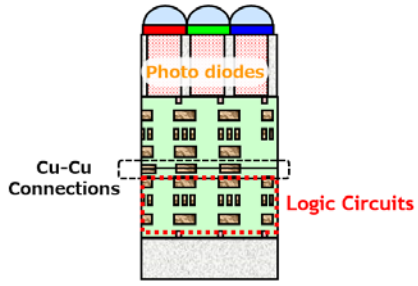

Fig. 4. Schematic diagram of a stacked BI-CIS with Cu-Cu connections

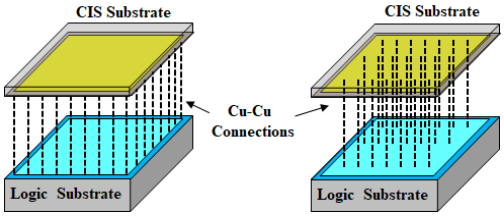

Fig. 5. Schematic diagrams stacked BI-CIS with Cu-Cu connections: peripheral connection (left)/ pixel-level connection (right)

The scaling of connection pitch is a key for high-performance 3D stacked devices. In order to realize further fine-pitch Cu-Cu connections the improvement of fabrication process is necessary: especially the misalignment of wafer stacking process could be critical to the electrical properties and reliabilities of the device. We have newly developed the wafer bonding process with better wafer alignment accuracy and successfully fabricated 3 µm-pitch Cu-Cu connections: the size of Cu connection pad is 1.5 µm square and the space between the adjacent Cu connection pads is 1.5 µm respectively [7].

Figure 6 shows a resistance distribution of the daisy chain module. The pitch of Cu-Cu connection is 3 µm, and the number of connections is 3M. The tight distribution shows good connectivity. Figure 7 shows the leakage current between different potential Cu-Cu connections in the module. The designed space between different potential adjacent Cu connection pads is 1.5 µm and the maximum misalignment value was 0.5 µm: therefore the actual minimum space between Cu connection pads is estimated to be 1.0 µm. It is shown that the leakage current is well suppressed even with the misalignment.

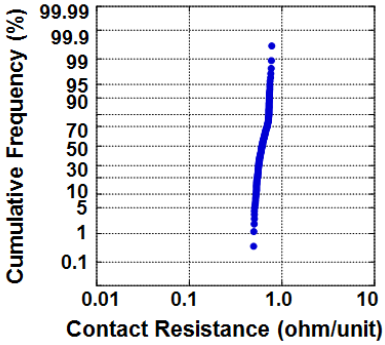

Fig. 6. Cumulative plot of contact resistance of each Cu-Cu connection

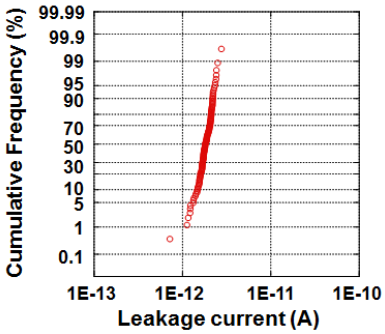

Fig. 7. Cumulative plot of leakage current between different potential Cu-Cu connections

IV. Conclusions

We have contributed to the development of multifunctional, high-performance products with various 3D chip stacking approaches. For the stacked BI-CIS, the TSV technology has been newly introduced to electrically connect upper and lower chips and it has contributed to enhance the functionalities. In recent year, for further fine-pitch and large-scale connections the Cu-Cu direct bonding technology has been developed and its connection pitch has been steadily shrunk. Thus, our newly developed 3D chip stacking technologies have been leading the evolution of 3D stacked semiconductor devices.

References

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