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A High Resolution Single Gold Proof-Mass CMOS-MEMS Accelerometer

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Abstract

This paper describes an implementation of a highly sensitive CMOS (complementary-metal-oxide semiconductor)–MEMS (microelectromechanical systems) capacitive accelerometer with a resolution below 100 μG (G = 9.8 m/s^2). To realize the high resolution CMOS-MEMS accelerometer, we optimize the structure of a gold proof-mass for the MEMS fabricated by the gold post-CMOS process and adopt a capacitive sensor circuit based on the relaxation oscillator in the 0.18 μm CMOS. The results of experiments confirm that the single gold proof-mass CMOS-MEMS accelerometer can obtain the resolution of 77 μG (total noise 44μG/√Hz, Brownian noise 92 nG/√Hz, the 4×4 mm^2 chip size) for a micro-G level sensing.

1. Introduction

CMOS-MEMS technology is an attractive method to realize a smaller module and a higher functionality regarding MEMS devices [1,2]. We have reported the sub-1 g CMOS-MEMS accelerometer [3] fabricated by the post-CMOS process using the multi-layer metal technology [4]. In this work, in order to establish the CMOS-MEMS accelerometer with the high resolution, we investigated the optimal thickness of the gold proof-mass for the MEMS accelerometer to reduce the Brownian noise (B_N) and adopted a capacitive sensor circuit [5] based on the relaxation oscillator in the 0.18 μm CMOS for the CMOS-LSI. The characteristics of the CMOS-MEMS accelerometer, the MEMS accelerometer, and CMOS circuits were experimentally evaluated, respectively.

2. Concept & Experiments & Results

A. CMOS-MEMS Concept

Figure 1 (a) shows a conceptual image of the gold proof-mass CMOS-MEMS capacitive accelerometer. The MEMS structure is freely formed on the CMOS circuit area by the multi-layer metal technology. Figure 1 (b) shows the circuit diagram of the capacitive sensor circuit in the 0.18 μm CMOS. The sensor circuits based on relaxation oscillators are suitable for the highly sensitive sensing because the circuits output time-domain data and time averaging can be used to reduce noise.

B. Analysis of Brownian Noise and Proo-mass Design

Figure 2 (a) shows B_N as a function of an effective proof-mass area including the etching hole area for removing a sacrificial film. In the case of being able to form the proof-mass thickness of 40 μm using the gold as the proof-mass material, the analysis results suggest that we can achieve the our target B_N below 100 nG/√Hz within a given chip area of 4x4 mm^2. Here, the Brownian noise B_N is given by

$$B_N = \frac{\sqrt{4k_B Tb}}{m}, \qquad [1]$$

where k_B, T, b and m are the Boltzmann constant (1.38×10^{-23} J/K), the absolute temperature, the viscous damping coefficient, and the proof-mass of an accelerometer, respectively. Based on the analysis results, we have proposed the MEMS accelerometer structure regarding the proof-mass as shown in Fig. 2 (b). The proposed proof-mass of MEMS accelerometer is formed by five layers of electroplated gold to realize the 40 μm thickness. The CMOS-MEMS accelerometer which consists of the proof-mass, the spring and the stopper is designed and fabricated by seven gold layers with the multi-layer metal technology.

C. Experimental Result

Figure 3 shows an SEM photographs of the chip and close-up view. It was found that the MEMS accelerometer was completely fabricated by the multi-layer metal technology[4]. Close-up details of the spring and the stopper are presented. We made the test board for measuring the CMOS-MEMS accelerometer as shown in Fig. 4 (a), (b). Figure 5 shows the experimental results of MEMS and CMOS-MEMS accelerometers. Figure 5 (a) shows the measured ring-down test to the MEMS accelerometer. It was evaluated by the laser doppler vibrometer (LV-1800, Ono Sokki), where the resonant frequency f_{res} and the quality factor Q were found to be 293 Hz and 11.4, respectively. The B_N obtained by the evaluation was 92 nG/√Hz. Figure 5 (b) shows the output period of the CMOS-MEMS accelerometer as a function of the input acceleration. We employed the vibration exciter (ASAHI SEISAKUSHO, WaveMaker05) to apply the acceleration to the CMOS-MEMS accelerometer. It was suggested that the CMOS circuit was operating correctly and the CMOS-MEMS accelerometer obtained the sensitivity of 0.306 μs/G at the power consumption of 13.2 mW. Moreover, in order to investigate the minimum resolution, we evaluated the Allan deviation by the experimental results of the noise characteristics at CMOS circuit and CMOS-MEMS accelerometer as shown in Fig. 6 (a), (b). The evaluation results confirmed that we can obtain the resolution of 37 aF and 77 μG in CMOS circuit and CMOS-MEMS accelerometer, respectively. As a result, the total noise of the CMOS-MEMS accelerometer was estimated to be the value of 44μG/√Hz. Device characteristics are summarized in Table I, where the measurement results are consistent with the design values.

3. Conclusion

We have implemented the high resolution single gold proof-

mass CMOS-MEMS accelerometer. Our proposed CMOS-MEMS accelerometer can realize the resolution of 77 μG obtaining the total noise 44μG/√Hz and B_N 92 nG/√Hz in the 4×4 mm^2 chip size**.** In conclusion, compared to our previous work and the other CMOS-MEMS accelerometers as shown in Fig.7 [2,3,6-10], it is confirmed that our proposed CMOS-MEMS accelerometer has a potential for achieving a higher resolution for a micro-G level sensing.

Acknowledgements

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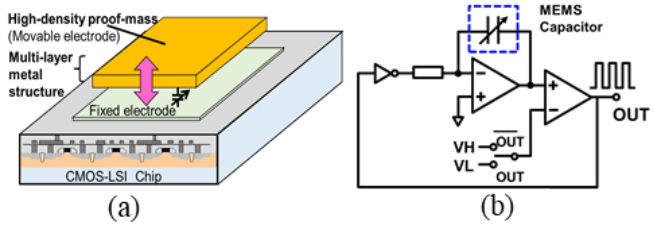

Fig.1 (a) The conceptual image of the proposed CMOS-MEMS accelerometer fabricated by the multi-layer metal technology. (b) The schematic diagram of the proposed sensor circuit.

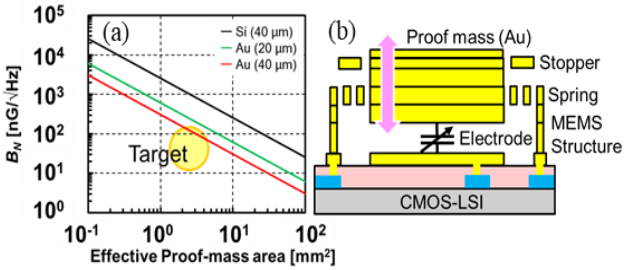

Fig.2 The analysis of the Brownian noise and the proof-mass. (a) The relationship between B_N and effective proof-mass. (b) The structure image of the proposed MEMS accelerometer.

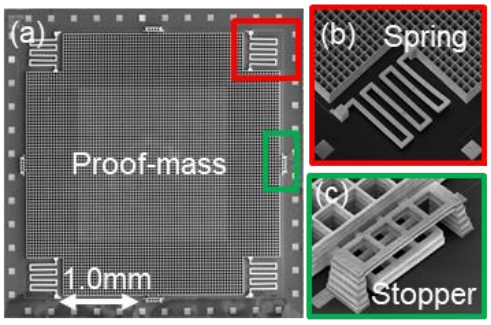

Fig.3 SEM photographs of the fabricated CMOS-MEMS accelerometer. (a) Chip view of CMOS-MEMS accelerometer. The proof-mass area is 3.3x3.3 mm^2. The MEMS structure is successfully fabricated by seven gold layers. Close-up images of (b) spring and (c) stopper.

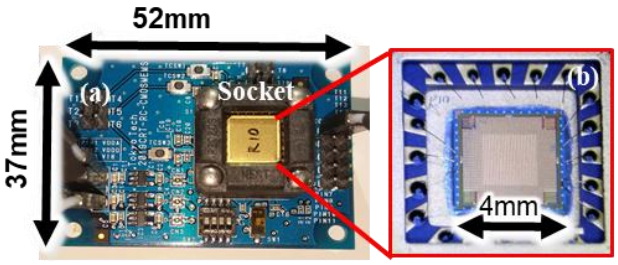

Fig.4 (a)Test board for measurement of CMOS-MEMS accelerometer. (b)CMOS-MEMS chip in ceramic 20 pin package.

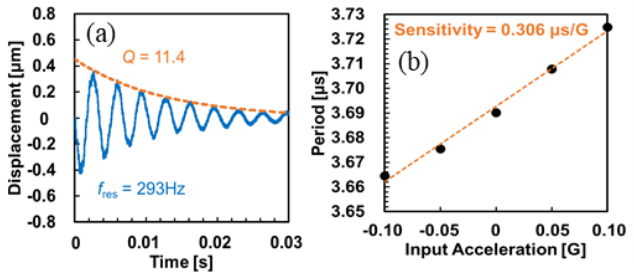

Fig.5 Experimental results. (a) LDV (Laser Doppler Vibrometer) measurement result of MEMS accelerometer. (b) Period output of CMOS-MEMS accelerometer as a function of input acceleration.

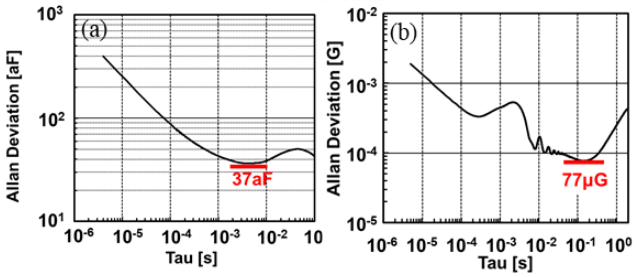

Fig.6 Allan deviation characteristics. (a) CMOS, (b) CMOS-MEMS accelerometer.

TABLE I Device characteristics.

Device	Parameters	Design	Measured
MEMS	Brownian B_N [nG/√Hz]	80	92
	Resonant frequency f_{res} [Hz]	267	293
CMOS-MEMS	Sensitivity [μs/G]		0.306

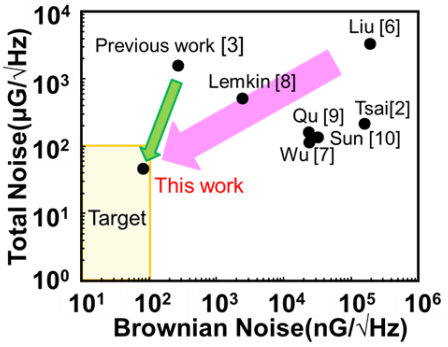

Fig.7 Comparison of CMOS-MEMS technology.