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Fabrication of Hollow Structure in Embedded Die Substrate for Heterogeneous Integration

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Abstract

The concept and fabrication of novel hollow structured embedded-die-substrate technology for micro electro mechanical systems (MEMS) applications are demonstrated. The CO_2 laser ablation is employed to remove resin used to embed a die in a cavity opened in a FR4 core substrate, followed by lamination of spacer and cap layers made of FR4. A chip in which piezo-resistance gauges were implemented was packaged to evaluate residual stress after each major process steps. A clear difference was observed in residual stress between two resin materials having a different coefficient of thermal expansion (CTE). The results indicate that the packaging technology is useful to minimize residual stress on the chip and to meet the requirement of miniaturizing package size.

1. Introduction

The demand on the package size miniaturization is rapidly growing, emphasizing application to advanced mobile communication and IoT. Electronics for these applications require the integration of the passive components and the active components for processing analog, RF, and digital signals in a package. The embedded die substrate technology is the most promising package structure to integrate these components [1]. However, in the conventional embedded die substrate, the die is fully covered by the substrate materials such as prepreg and resin [2, 3]. This fact imposes a severe limitation for the application to such components as micro electro mechanical systems (MEMS) sensors, bulk acoustic wave resonator (BAW) filter, or surface acoustic wave (SAW) filter whose performance is highly sensitive to the mechanical stress.

In this paper, we propose and demonstrate the fabrication of a hollow structure in the embedded die substrate. The effectiveness of the hollow structure is evaluated by applying the process to the packaging of a test chip having piezo-resistance gauges and measuring residual stress on it.

2. Structure and Fabrication Process

The schematic structure of the embedded die substrate having the hollow structure is shown in Fig. 1. A chip is embedded in the substrate. In the conventional die embedded substrate, the chip is fully covered with foreign materials. In contrast, the hollow structures are formed at both the top and bottom sides of the chip. The chip is held with resin filled at the periphery of the chip. The chip is interconnected to the outer pad through the redistribution layer (RDL). Ajinomoto Build-up Film (ABF) is used for the resin.

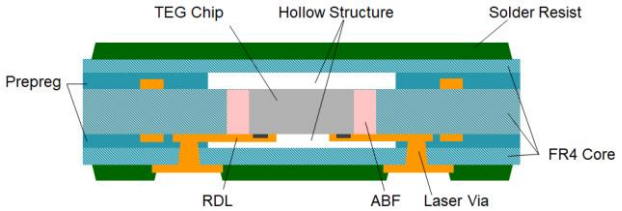

Fig. 1 Schematic structure of the embedded die substrate with a hollow structure.

Figure 2 shows a schematic of the fabrication process flow of the hollow structure in the substrate. A test element group (TEG) wafer of the piezo-resistance gauge chip was thinned down to 150 μm-thick. A 6 μm-thick Cu backside metal (BSM) was electroplated to protect the chip from CO_2 laser irradiation employed in the process. Then, the TEG wafer was diced into 3.0×3.0 mm^2 chips. The embedded die process is started with the preparation of the through-hole cavity in the core frame of 150 μm-thick FR4 (MCL-M- 679FG, Hitachi Chemical). The through-holes for global alignment marks were formed by mechanical drilling. The alignment mark for the die-attach process was patterned using a subtractive patterning process. The through-hole cavity for the die embedding was mechanically drilled by the router. The single-sided adhesive tape was then laminated from the bottom side of the frame. The TEG chip was placed on the tape with face down using a flip-chip bonder.

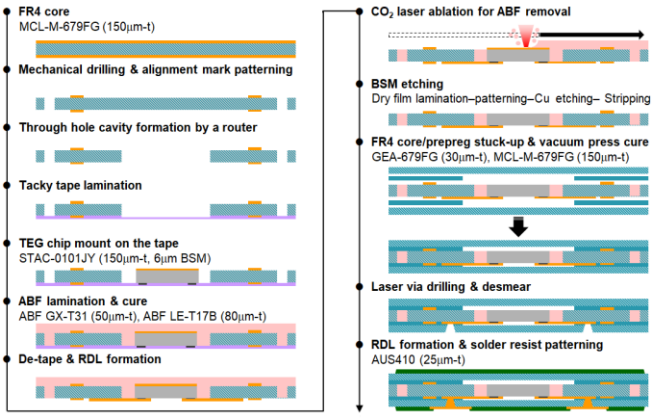

Fig. 2 Schematic fabrication process flow of the embedded die substrate for the hollow structure.

Two kinds of ABF, GX-T31 (50 µm-thick, CTE: 23 ppm/K) and LE-T17B (80 µm-thick, CTE: 7 ppm/K), were tested as the cavity filling material to compare the residual stress during assembly. ABF was laminated by the vacuum laminator at 120 ℃ for 30 sec, followed by curing at 100 ℃ for 30 min and 190 ℃ for 60 min. The single-sided tape was then peeled off. A 6 µm copper RDL with the titanium and copper seed layer was plated by a semi-additive process (SAP). The remaining ABF layer on top of the FR4 core frame layer was removed by the CO_2 laser ablation. The exposed BSM was selectively etched off by copper etching etchant using the patterned dry film as a mask. The embedded die after BSM etching is shown in Fig. 3.

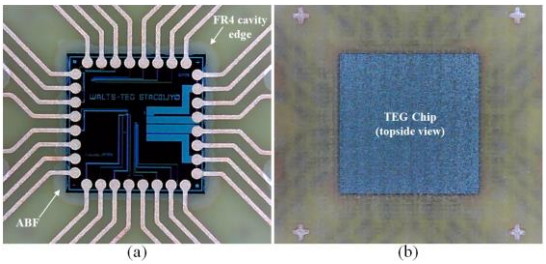

Fig. 3 The embedded die after the BSM etching process; a) the bottom side of the die and b) the top side of the die.

A 30 µm thickness prepreg (GEA-679FG, Hitachi Chemical) was used as an adhesion layer for build-up. 7.0×7.0 mm^2 cavity was mechanically formed by the router to the prepreg to eliminate the risk of the resin bleed out on the die from the prepreg. The prepreg was stacked up from both sides with a 150 µm FR4 core. The vacuum press cure at 185 ℃ for 2.5 hours was applied for the final cure. After the build-up, the CO_2 laser irradiation was conducted to make via holes, followed by a standard desmear process to remove a smear. The outer pad was formed by SAP using the seed layer of electroless copper plating. The film type of solder mask with 25 µm-thick (AUS410, Taiyo Ink) was laminated. Then, the substrate was singulated as a 12×12 mm^2 package size for the cross-section analysis. The cross-section view with a scanning electron microscope (SEM) is shown in Fig. 4. The hollow structure was clearly formed on the top and bottom sides of the embedded die. The gap between the FR4 and the die was 28.4 µm at the top side and 22.0 µm at the bottom side.

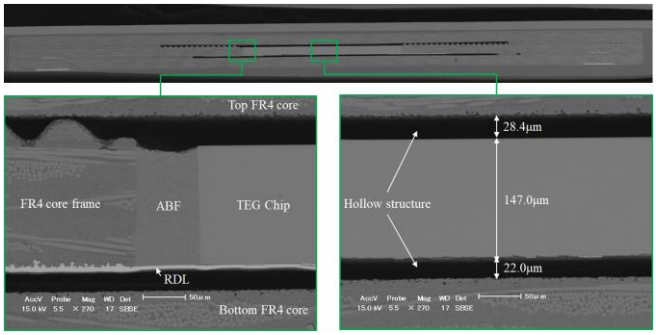

Fig. 4 Cross-section SEM image; a) the edge of the embedded die and b) the center of the embedded die.

3. Residual Stress Measurement

The residual stress was evaluated from the change in resistance of the piezo-resistance gauge from the value measured before assembly. The four-terminal method was used to measure resistance. The sensitivity data of the wafer supplier was used to convert from resistance to stress [4]. Figure 5 shows the measured results of the residual stress. The induced stress during assembly is generally occurred due to CTE mismatch among the material. The large tensile stress was observed after ABF cure for both samples. This is due to the shrinkage of ABF on the chip. The structure at this step is similar to the conventional die embedded substrate. The stress was released after the removal of ABF. The removal of BSM also releases stress. It is clear that the LE-T17B, which has smaller CTE than GX-T31, shows much less stress. After the solder mask, the residual stress was changed again. Nevertheless, the residual stress was kept much lower in the LE-T17B sample.

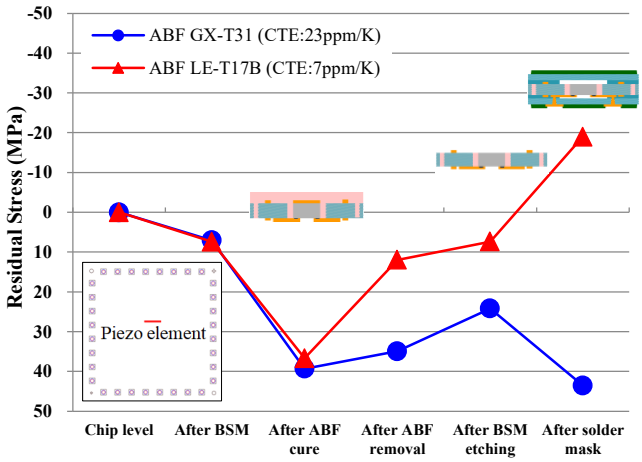

Fig. 5 Change in residual stress with the progress of process steps.

4. Conclusions

We demonstrated a new approach to the fabrication of the hollow structure in the embedded die substrate packaging technology. Experimental results clearly indicated the effectiveness of the formation of hollows at both sides of the chip to reduce residual stress. It is also suggested that the adjustment of CTE of the resin will make zero-stress packaging possible. This technology will be useful for heterogeneous integration.

Acknowledgments

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