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Novel Enhancement-Mode Tri-Gate InAlN/GaN Tunnel-Junction HEMT

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Abstract

We demonstrate a high performance enhancement-mode (E-mode) tri-gate InAlN/GaN tunnel-junction HEMT. Through a source Schottky tunnel-junction (SSTJ) controlled by a tri-gate structure, a positive threshold voltage (V_{TH}) of +0.8 V is realized. The proposed device also reveals excellent electrical performances, including a maximum drain current ($I_{D,\,max}$) of 508 mA/mm, on-state/off-state current (I_{on}/I_{off}) ratio of 10^9-10^{10}, subthreshold swing (SS) of 72 mV/decade, and specific on-resistance ($R_{on,\,sp}$) of 0.98 mΩ·cm^2. Moreover, the SSTJ combined with the tri-gate structure exhibits a superior breakdown voltage (V_{BD}) of 730 V. These results indicate great potential for high power device applications.

1. Introduction

GaN high electron mobility transistors (HEMTs) feature a lot of superior material properties, including high electron mobility, wide band-gap, and large breakdown field. These properties are very suitable for power electronics applications. Considering safety design in the power electronic systems, high performance enhancement-mode (E-mode) GaN HEMTs are required. Tri-gate (FinFet) structure has recently been applied to GaN HEMTs for E-mode devices. However, a conventional tri-gate (FinFet) GaN HEMT requires very small channel widths to achieve a E-mode HEMT, which needs very critical process conditions and could cause the on-resistance (R_{on}) to be degraded [1]. In this study, a tri-gate InAlN/GaN HEMT combined with a source Schottky tunnel-junction (SSTJ) is demonstrated. It doesn't require very small channel widths to achieve a E-mode HEMT while having excellent performances.

2. Device Fabrication

The InAlN/GaN heterostructure was grown on a 6-inch silicon wafer by metal organic chemical vapor deposition (MOCVD). The heterostructure consisted of 9-nm InAlN barrier layer, 1-nm AlN spacer layer, 300-nm GaN channel, and 3.5-μm GaN buffer layer. The 2DEG density and electron mobility are 2.2×10^{13} cm^{-2} and 1018 cm^{2}V^{-1}s^{-1}, respectively. The schematic and TEM images of the proposed devise are shown in Fig. 1. The device fabrication started with the mesa isolation and fin structure by using inductively coupled plasma reactive ion etching (ICP-RIE) with a BCl_3/Cl_2 gas mixture. A metal stack of Ti (20 nm)/Al (100 nm)/Ni (40 nm)/Au (100 nm) was evaporated and annealed at 900 °C in ambient N_2 for 30 s to form the drain ohmic contact. In order to form the SSTJ, an about 7-nm-deep source recess was first etched by low power Cl_2-based ICP-RIE. Subsequently, Ti (25 nm)/Au (100 nm) was deposited at the source region. Finally, 20-nm Al_2O_3 as the gate dielectric layer was deposited by ultrasonic spray pyrolysis deposition (USPD) [2], and Ni/Au was evaporated to form the gate. Note that the gate was partially overlapped with the source Schottky contact, as shown in Fig. 1(b). The overlap length (L_{OL}) is 0.2 μm.

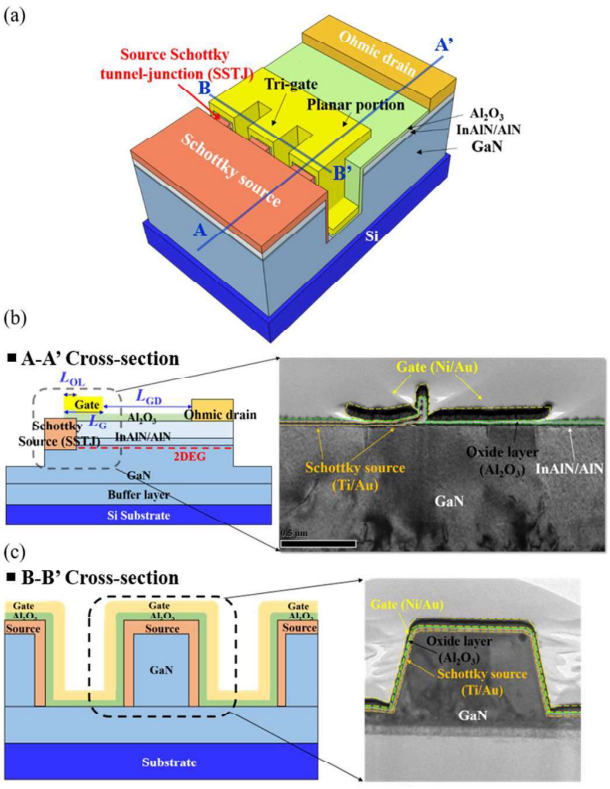

Fig. 1. (a) 3D schematic illustration of the proposed E-mode tri-gate InAlN/GaN tunnel-junction HEMT. (b) A-A' cross sectional schematic and transmission electron microscopy (TEM) image of the SSTJ. (c) B-B' cross sectional schematic and TEM image of the SSTJ. (The fin width and height are about 500 and 400 nm, respectively.)

Fig. 2 shows a simplified model for the operating principle of the E-mode tri-gate tunnel-junction device. The source region of the device forms a Ti-based Schottky junction. As the gate is applied to a negative voltage or zero voltage, the carriers are difficult to tunnel through the Schottky barrier due to the large Schottky barrier width (SBW), as shown in Fig. 2's label A and B. This can make the device shut down (off-state) and greatly reduce the occurrence of leakage current. As the gate is gradually applied to a positive voltage, the conduction band of GaN is pulled down, which effectively reduces the SBW (as shown in Fig. 2's label C), making the tunneling current significantly increase and the device turn on (on-state) [3]. The tri-gate structure can enhance the gate controllability for the SSTJ, further improving device performances.

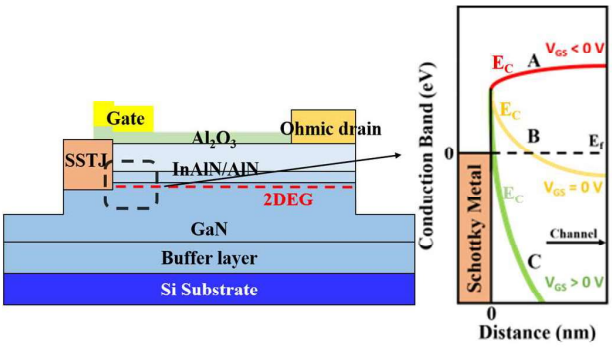

Fig. 2. Schematic illustration of a simplified model for the operating principle of the SSTJ.

3. Results and Discussion

The transfer and output characteristics of the devices are shown in Fig. 3(a) and 3(b). The threshold voltage (V_{TH}) of the tri-gate tunnel-junction device is about 0.8 V at V_{DS} = 10 V, which is about 4.0 V higher than the reference planar device. The maximum drain current ($I_{D,\,max}$) of the proposed device is 508 mA/mm (at V_{GS} = 5 V and V_{DS} = 10 V). Moreover, the E-Mode tri-gate tunnel-junction device has superior characteristics such as a steep SS of 72 mV/decade, I_{on}/I_{off} ratio of 10^9-10^{10}, and I_{off} of about 10^{-7} mA/mm. Compared with the reference planar device, the obvious improvements of the proposed device are mainly attributed to the SSTJ combined with the tri-gate structure [3], [4]. The R_{on} of the proposed device is 10.5 Ω·mm, extracted from the I_D-V_{DS} curve at V_{GS} = 5 V and V_{DS} = 1 V. The specific R_{on} ($R_{on,\,sp}$) is 0.98 mΩ·cm^2, calculated from 6.5-μm L_{SD} and 1.5-μm transfer length for each contact.

Three-terminal off-state breakdown voltage (V_{BD}) characteristics are shown in Fig. 4. It is found that the value of V_{BD} of the proposed tri-gate InAlN/GaN tunnel-junction device reaches 730 V at V_{GS} = 0 V with a floating substrate. The high V_{BD} of the proposed device results from two reasons. First, the leakage current through the buffer layer can be suppressed because the source/buffer junction is an inherently reverse-biased Schottky junction in the off-state [3]. Second, the gate consists of the tri-gate portion and planar portion (as shown in Fig. 1(a)). The planar portion acts similar to an inherently integrated field plate (FP) due to the pinch-off voltage differences between the tri-gate portion and planar portion [5], [6]. This can provide effective edge termination and improve the V_{BD}.

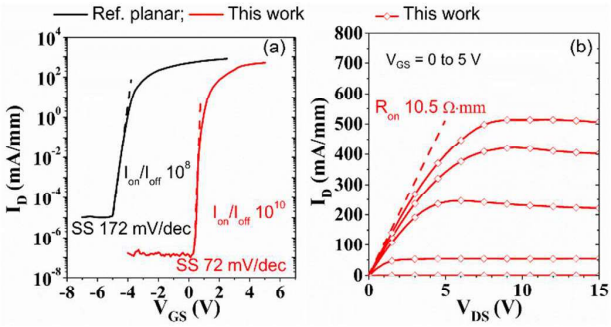

Fig. 3. (a) Transfer characteristics of the proposed device and reference planar device. (b) Output characteristics of the proposed device. The gate length (L_G) and gate-to-drain length (L_{GD}) are about 1.5 and 5 μm, respectively.

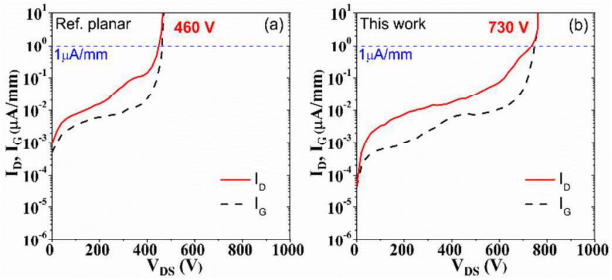

Fig. 4. Off-state breakdown characteristics of (a) the proposed device (V_{GS} = 0 V) and (b) the reference planar gate device (V_{GS} = -7 V). The gate length (L_G) and gate-to-drain length (L_{GD}) are about 1.5 and 5 μm, respectively.

4. Conclusions

In this study, a novel high performance E-mode InAlN/GaN MOSHEMT on silicon has been successfully demonstrated. The device exhibits the excellent characteristics, including SS, I_{off}, and I_{on}/I_{off} ratio due to the SSTJ controlled by tri-gate structure. Additionally, the proposed device also reveals a high V_{BD} of 730 V. These results suggest that the proposed device design has great potential for the power electronics industry.

Acknowledgements

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