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Bayesian optimization and expected hyper volume improvement for SiO_2/GaN capacitor

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Abstract

We present an optimized fabrication process using Bayesian optimization and Expected Hyper Volume Improvement (EHVI) method with the goal of reducing interface state density (D_{it}) and fixed charge (Q_{eff}) in SiO_2/GaN metal-oxide-semiconductor (MOS) capacitor. The MOS capacitor fabricated through the above method was evaluated by capacitance and conductance. In this study, the deposition conditions of plasma-enhanced chemical vapor deposition for the SiO_2 film were optimized. As a result, the reduction of Q_{eff} and D_{it} in SiO_2/GaN MOS capacitors was achieved by the proposed method. These results revealed the effectiveness of Bayesian optimization and EHVI in determining the optimized fabrication process.

1. Introduction

The interface quality of insulator/GaN is critical in GaN power device. There are many reports on the SiO_2/GaN interface and SiO_2 quality on the GaN [1,2,3]. But the ideal insulator/GaN interface has not yet been revealed. Recently, materials informatics has become active [4,5]. We proposed to apply Bayesian optimization and Expected Hyper Volume Improvement (EHVI) for SiO_2/Si metal-oxide-semiconductor (MOS) capacitor fabrication to get better quality MOS capacitor such as lower interface state density(D_{it}) and the fixed charge (Q_{eff}) with minimal process trial. In this study, we used the above combination to optimize SiO_2 deposition conditions. From the results, we confirmed that the combination of Bayesian optimization and EHVI is effective for the fabrication process optimization.

2. Experiment method

N-type GaN substrate was used for MOS capacitor. Prior to the SiO_2 deposition, the substrates were cleaned by buffered-HF and HCl. Plasma-enhanced chemical vapor deposition (PECVD) with TEOS and O_2 was used to deposit SiO_2 film (thickness: ~ 80 nm). After that, thermal heating evaporation system provided Al top and bottom electrodes. Finally, N_2 gas annealing was performed at 400°C for 30 min as a post metallization anneal (PMA). After the PMA, capacitance-voltage (C-V) measurements were performed to evaluate electrical properties. The conductance method estimates D_{it}. A shift from the theoretical C-V curve gives us Q_{eff}. After the measurement, the deposition conditions of the SiO_2 film on GaN were optimized. At this time, temperature, pressure, RF power, TEOS flow rate, O_2 flow rate of PECVD were divided into 30 equal parts. This condition was optimized by Bayesian optimization. After Bayesian optimization, we selected the conditions of PECVD by using EHVI.

3. Results

The first SiO_2 deposition conditions were chosen by Latin Hypercube sampling. According to the results (Fig. 1), we found a relationship between D_{it} and Q_{eff}. D_{it} decreased by increasing the pressure, RF power, TEOS flow rate and O_2 flow rate. Based on these results, we optimized SiO_2 deposition condition by Bayesian optimization and EHVI (Fig. 2). Blue points are the experimented results of SiO_2/GaN MOS capacitor. Green points are the optimized results by Bayesian optimization from blue points. Pink points are chosen by HEVI from green points. After the optimization, we found the condition which achieved conductance decrease and D_{it} decrease (Fig. 3,Table. 1). As a result of measuring the MOS capacitor fabricated in this process by the conductance method, the D_{it} of the MOS capacitor was 7.9×10^{11} $eV^{-1}cm^{-2}$ at first time without optimization. The D_{it} of MOS capacitor with optimization is 4.1×10^{10} $eV^{-1}cm^{-2}$. The C-V characteristic was analyzed between ideal curve and measured curve with 1 MHz signal (Fig. 4). These results indicate that the combination of Bayesian optimization and EHVI can be effective method to decrease the D_{it} of MOS devices.

4. Conclusions

By working on Bayesian optimization and HPVI to fabricate GaN MOS capacitor with good characteristics. This optimization method can be applied to fabricate other devices.

References

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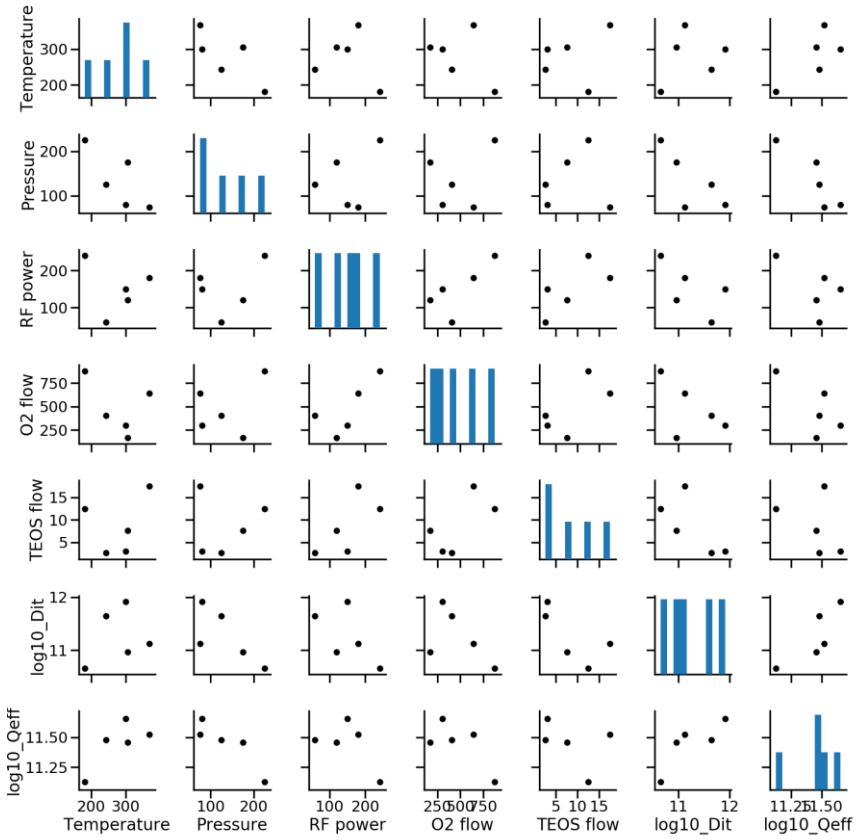

Fig.1 Result of relationship between Dit and deposition condition

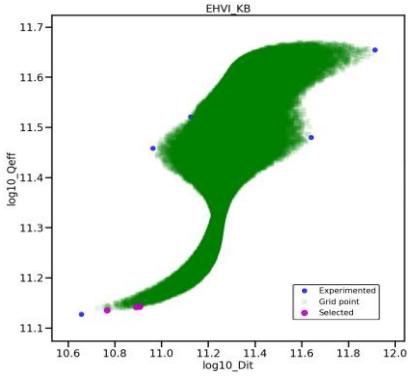

Fig.2 Grip point after Bayesian optimization.

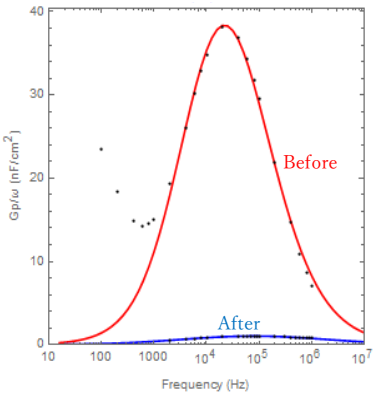

Fig.3 G-V characteristic before and after the optimization.

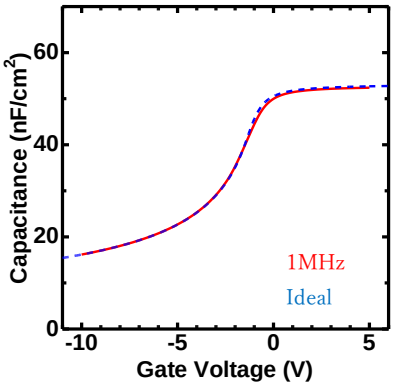

Fig.4 C-V characteristic of SiO_2/GaN MOS capacitor after the optimization

Table 1. SiO_2 deposition condition before optimization and after optimization

	Temperature[℃]	Power[W]	Pressure[Pa]	TEOS[sccm]	O_2[sccm]
Before the optimization	300	150	80	300	3
After the optimization	200	238	240	903	12.8