

Backside Integration of III-V/Si Hybrid Laser in a Si-SiN Photonics Platform

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Abstract

We report on the fabrication and characterization of multilevel Si/SiN/III-V transmitter circuits. The III-V material is heterogeneously integrated on the backside of the SOI layer in order to make hybrid laser sources. We show single mode operation of a Si/III-V hybrid laser. The chip output is performed via a specially designed backside SiN-Si grating coupler. This result validates the first integration of III-V on the backside of a Si/SiN platform.

1. Introduction

The constantly growing network traffic in data centers requires low cost, high speed and energy efficient transmission solutions [1], [2]. Integrating SiN, a low thermal coefficient material, in a photonics platform allows the realization of wavelength multiplexers with low temperature sensitivity [3], reducing the power consumption of the thermo-electric controllers placed at the packaging level. A Si/SiN platform is therefore an attractive solution to make energy efficient high data rate optical transceivers [4]. On the other hand, integrating III-V material on Si for hybrid laser sources [5], [6] and electro absorption modulators reduces packaging complexity and improves the scalability to a larger number of channels. However, the co-integration of Si, SiN, and III-V is challenging, as it requires several wafer bondings [7]. Depending on the integration path, some part of the fabrication has to be done on the wafer backside (the design of hybrid laser cavities dictates that Si and III-V are less than 150nm apart for efficient optical coupling). Furthermore, when a multi-level backend-of-line (BEOL) is needed for example for the RF connection of the high frequency modulator, the integration of the laser source on the backside of the wafer is mandatory [8].

2. Fabrication

The starting material is a set of 200mm Silicon-on-Insulator wafers. Si (300nm-thick) and SiN (600nm-thick deposited by Plasma Enhanced Chemical Vapor deposition) are first patterned on the wafer frontside. Then a carrier substrate is bonded (intermediate cross section Fig. 1 a), wafers are flipped and the original substrate is removed. The process is resumed on the backside with an amorphous silicon thickening step (500nm-thick Si is necessary for a good III-V/Si effective index matching). The associated patterning step includes feature sizes down to 120nm thus requiring the use of

193-nm UV photolithography with frontside-backside alignment. Notably, the SiN and the amorphous silicon are deposited at low temperature (<350°C) making the process compatible with the BEOL. The multi-quantum well III-V substrate is bonded on the back of Si and patterned. A total of 12 backside patterning levels is necessary to complete the fabrication (final cross section in Fig 1 b and SEM image in Fig. 2 a).

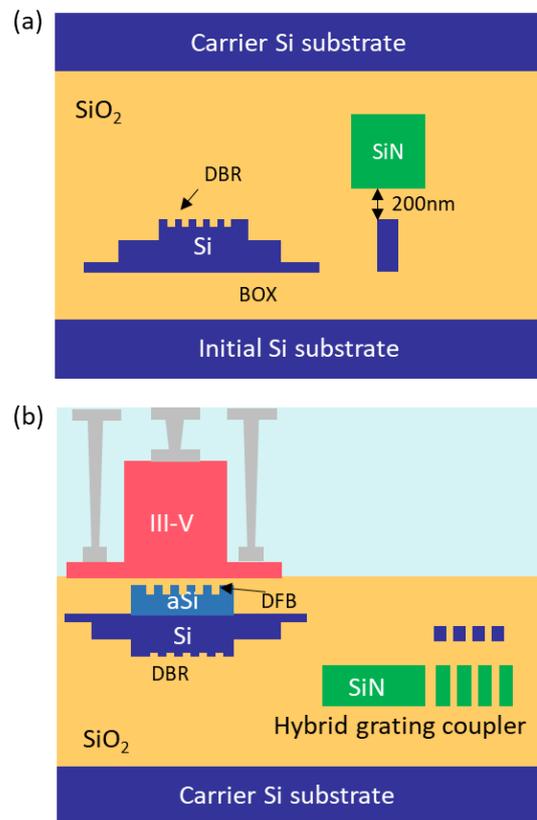


Fig. 1 (a) Cross section schematics at the end of the frontside fabrication, before flipping the wafer. (b) Final cross section with III-V on the backside.

3. Results

The Si/SiN platform includes a Coarse Wavelength Division Multiplexing (CWDM) SiN multiplexer based on Echelle gratings and a SiN/Si hybrid grating fiber coupler specially designed for backside coupling and featuring a 50nm (-1 dB) bandwidth (see also [4]). We show the operation of a Distributed FeedBack (DFB) laser (Fig. 2 b). The laser

shows a single mode at 1312nm with a side mode suppression ratio of 44dB and an estimated output power (in the waveguides) of 0.8mW. Notably, the hybrid DFB laser is coupled to a SiN waveguide and the chip output is performed through the backside SiN/Si grating fiber coupler. This demonstration is the first realization of a III-V/Si hybrid laser on the backside of an Si/SiN platform.

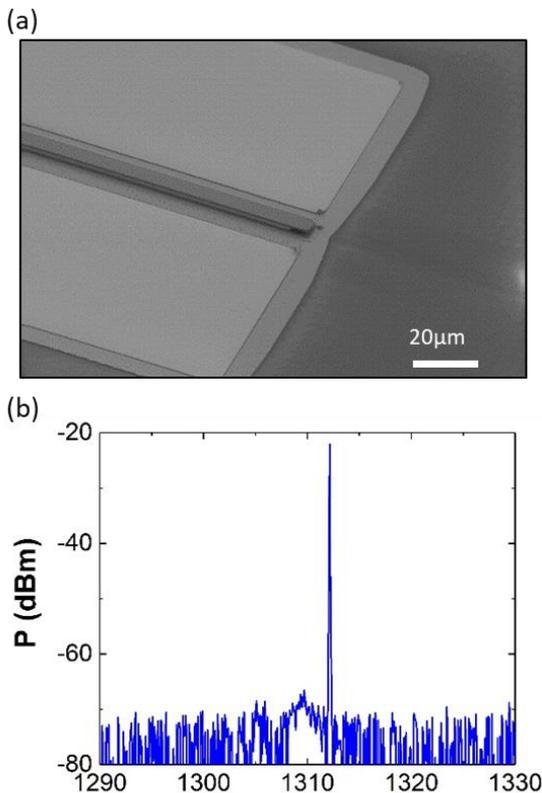


Fig. 2 : (a) Electronic microscope image of the III-V gain section. (b) Si/III-V DFB laser spectrum.

4. Conclusion and perspective

The fabrication of III-V structures on the backside is a promising integration path for wafers coming from industrial foundries with a stabilized process flow: the III-V integration can be done on the backside of 300mm wafers, without any stack modification while remaining CMOS compatible.

Acknowledgements

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