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Design of an Organic SRAM Cell with p-type Access Transistors

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***Abstract*—We propose an organic SRAM cell that is suitable for the implementation using low voltage organic thin-film transistors (OTFTs). Replacing n-type OTFTs, we use p-type OTFTs for the access transistors to gain higher area efficiency and better robustness than conventional SRAM structures. The stability of the proposed SRAM cell has been optimized through SPICE simulations, and experimental measurements confirmed the correct and stable operation of the proposed SRAM cell.**

1. Background

The organic thin-film transistors (OTFTs) bring new benefits, such as flexibility, lightness and decomposability in electronic design. In addition, the organic circuits can be fabricated on flexible materials through low-cost and low-temperature printing processes. Therefore, various applications such as RFID tags [1], microprocessors [2] and sensors [3] have been reported. The static random access memory (SRAM) is an essential component of these electronic systems for storing data or instructions. However, due to the significant difference in the strength of n-type and p-type OTFTs, conventional SRAM design developed for silicon technology may not be applied as is.

In this paper, we propose a novel construction of an SRAM cell that is suitable for the implementation using low supply voltage OTFTs. As shown in Fig. 1, the proposed SRAM cell uses p-type OTFT to simultaneously achieve high area efficiency and stable operation.

2. SRAM and its operation

The standard 6-transistor (6T) SRAM cell consists of a pair of cross-coupled inverters that stores a state, and a pair of access transistors to control read and write operations.

In the read operation, the bitlines are initially precharged as floating logical "1." Assume node Q is "0" and Q_b is "1." When the wordline is raised, $bit1$ should be pulled down through A1 and D1. Due to the charge stored in the bitline and the current flowing in through A1, node voltage of Q tends to rise while Q is held low by D1. For successful read operations, D1 must be stronger than A1. In the write operation, we again assume Q is initially 0 and wish to write 1 to node Q. The cell must be written by forcing Q_b low through A2. To pull Q_b low enough, P2 must be weaker than A2.

The stability of SRAM cells is quantified by the static noise margin (SNM) in different mode of operations. The test circuits for determining the SNM are shown in Fig. 2. The SNM is determined by the length of the side of the largest square contained in the butterfly diagram [4]. According to the above read and write stability constraints, in standard SRAM cells, n-type pull-down transistors must be designed strongest among all. The n-type access transistors are of intermediate strength, and p-type pull-up transistors must be the weakest. In the case of OTFTs, because the n-type OTFTs are generally much weaker than p-type, the size of n-type access transistors has to be extremely large, which significantly increases the cell area. To avoid using weak n-type OTFTs, a pseudo-CMOS topology configured with only p-type OTFTs has been proposed [5], but the noise margin remains limited.

3. Organic SRAM cell with p-type access transistors

We propose a new SRAM cell that occupies smaller area and achieves higher stability than conventional ones. In our cell, instead of using n-type access transistors, we use p-type access transistors. With this construction, the relative strength constraint in pull-down, access, and pull-up transistors are easily satisfied, without increasing transistor sizes significantly. Moreover, the writability in this structure is not a design challenge, since p-type transistors is naturally stronger than n-type in our OTFTs. Note that the proposed SRAM cell uses "0" precharge at the beginning of the read operations.

In order to attain stability of the proposed SRAM, the SNM in hold and read state is firstly simulated by sweeping the transistor sizes: the ratio of pull-down to pull-up transistor size ($\beta_{\rm pd} = W_{\rm D}/W_{\rm P}$ where $W_{\rm X}$ is the channel width of transistor X), and that of access to pull-up transistor sizes ($\beta_{\rm ac} = W_{\rm A}/W_{\rm P}$). The OTFT models used in the simulation is fitted to the devices implemented in this work. Considering the strengths of the transistors, $\beta_{\rm pd}$ is varied from 0.4 to 20 and $\beta_{\rm ac}$ is varied from 0.2 to 2 in this simulation. The results of SNM in hold and read state at 3 V supply voltage are shown in Fig. 3. The SNM is positive for all the combination of $\beta_{\rm pd}$ and $\beta_{\rm ac}$, meaning that the proposed SRAM can operate stably under large characteristic variations. In hold state, the SNM is constantly above 1 V and increases as $\beta_{\rm pd}$ increases. In the read state, the $\beta_{\rm ac}$ is a definitive factor. A small $\beta_{\rm ac}$ is required for stable read operation. Desirable space for stable operation is shown in Fig. 3.

In the case of conventional SRAM cells with n-type access transistors, it is necessary to consider writability. The simulation results are shown in Fig. 4. For stable operation, the $\beta_{\rm pd}$ needs to be about 6 and $\beta_{\rm ac}$ should be 10 or higher. Meanwhile, the proposed SRAM structure with $\beta_{\rm pd} = 0.75$, $\beta_{\rm ac} = 0.5$ and pull-up transistors with $W/L = 1200/50\,\mu$m is chosen for the fabrication and measurement. Under the condition that the minimum transistor size is the same, the area of the proposed SRAM reduced by 75% compared to the existing circuit.

4. Measurement Results

The $I_{\rm d}$-$V_{\rm g}$ characteristics of five OTFTs used in this work are measured first, as shown in Fig. 5. The p-type and n-type semiconductors are pentacene and TU-1, respectively. The OTFTs possess on-off ratio of 300 and 700 for p-type and n-type, respectively. As expected, p-types are about 10x stronger than n-types, on average. The microphotograph of the test chip and the measured SNMs at 3 V supply voltage in hold and read states are shown in Fig. 6. Though n-type OTFTs are weak, positive SNM has been observed owing to

the relatively small off-current of p-type OTFTs. The read and write operations are verified in Fig. 7. Read operations are performed after writes. In read operation, the bitlines are firstly precharged to 0 V, and the wordline is asserted. To confirm the successful read operation, bitlines are connected with 0.1 μF capacitors. With these results, we can see that the correct write/read operation of the proposed SRAM cell has been confirmed. The power consumption for a read and a write operation is 50.2 nW and 33.2 nW respectively.

5. Conclusion

In this work, we proposed a schematic of SRAM with p-type access transistors, which is suitable for characteristic of OTFTs. The area of the proposed SRAM reduced by 75% compared to the existing circuit. Through the simulation and measurement of the organic SRAM, we confirm that the proposed SRAM can operate stable.

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References [1] H. Marien, et al., IEEE J. Solid-State Circuits, pp. 276–284 (2011). [2] K. Myny, et al., IEEE J. Solid-State Circuits, pp. 284–291 (2012). [3] M. Islam, et al., IEEE JETCAS pp. 81–91 (2017). [4] E. Seevinck, et al., IEEE J. Solid-State Circuits pp. 748–754 (1987). [5] M. Takamiya, et al., IEEE J. Solid-State Circuits, pp. 93–100 (2007).

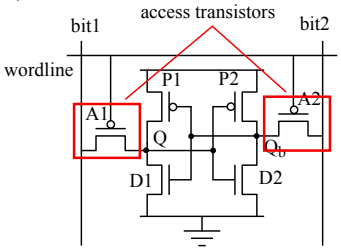
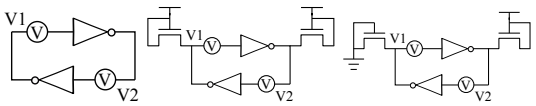
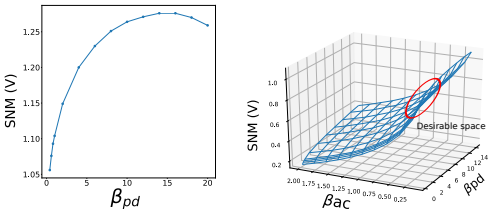


Fig. 1: Circuit schematic of the proposed 6-transistor (6T) SRAM with a pair of p-type access transistors. Compared with the conventional SRAM cell, n-type access transistors are replaced with p-type OTFT.



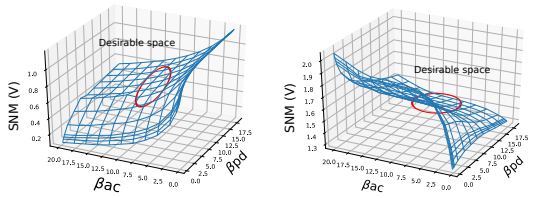
(a) Hold state (b) Read state (c) Write state

Fig. 2: The test circuits for deriving static noise margin (SNM). SNM is determined by length of the side of the largest square in butterfly diagram drawn by changing V1 and V2.



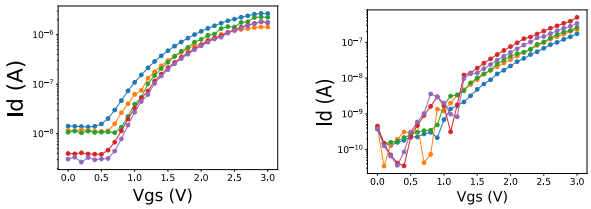
(a) hold state (b) Read state

Fig. 3: Optimization of transistor sizes with SNM in hold and read states at 3 V supply voltage. β_{pd} is swept from 0.4 to 20 and β_{ac} is swept from 0.2 to 2. Simulation model parameters are based on device measurements in this work.



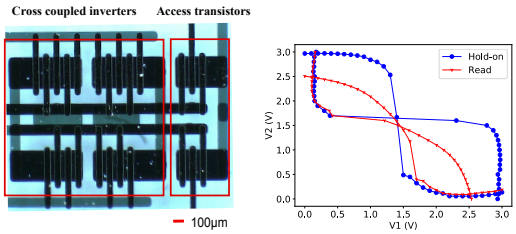
(a) Read state (b) Write state

Fig. 4: Simulation results for conventional SRAM structure for finding optimal transistor sizes in read and write SNM at 3 V supply voltage. β_{pd} and β_{ac} are swept from 0.4 to 20.



(a) p-type (b) n-type

Fig. 5: Measured I_{d}-V_{g} characteristics of OTFTs using the same process with the proposed SRAM. L and W of the devices are 50 and 1200 μm, respectively.



(a) Microphotograph (b) Measured SNM

Fig. 6: Test chip microphotograph and the measurements of SNM in hold-on and read states.

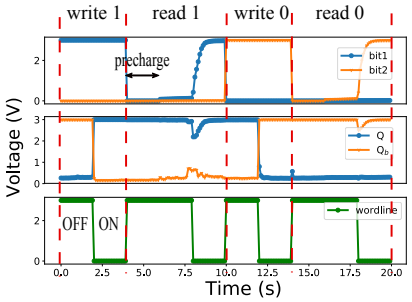


Fig. 7: Write and read operation of the proposed SRAM cell. In each operation, the access transistors are first turned off and then turned on to confirm the operation of the wordline. In read operation, the bitlines are precharged to 0. To confirm read operation clearly, bitlines are connected with 0.1 μF capacitors.