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Selective-area growth of InGaAs/GaSb core-shell nanowires on Si

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Abstract
InGaAs and GaSb have attracted channel materials as next-generation field-effect transistors because they have high carrier mobilities. However, challenge is remained in forming atomically smooth GaSb layer due to huge surfactant effect of Sb atoms. Here we repot on selective-area growth of vertical InGaAs/GaSb core-shell nanowires on Si(111).

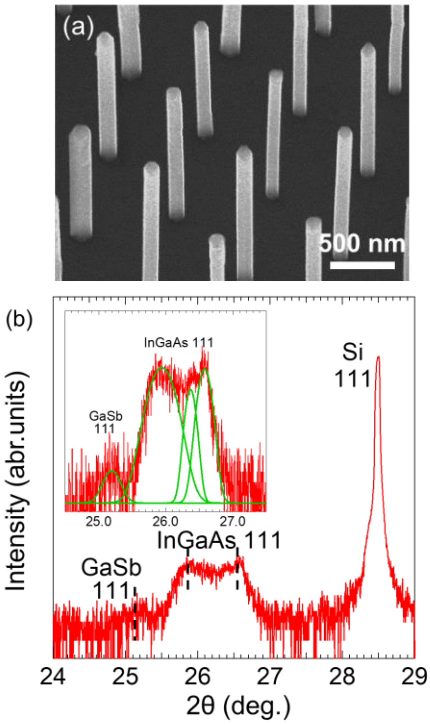
1. Introduction
III-V compound semiconductor nanowires (NWs) have attracted materials as next-generation nanoelectronics. In particular, indium gallium arsenide (InGaAs) and gallium antimonide (GaSb) are expected as channel materials for high-performance field effect transistors (FETs) due to high carrier mobility [1]. InGaAs/GaSb system is good candidate for the tunnel junction for low-power switching device. There is, however, still difficulty in versatile epitaxy of Sb-based III-Vs due to surfactant effect of Sb atoms. With this regard, NW smooth facets can be utilized for forming a smooth GaSb layer. Moreover, the abrupt interface between InGaAs and GaSb is of important to take advantage of tunnel FET because the interface enhances tunnel current. In this paper, we investigated selective-area growth of InGaAs/GaSb core-shell (CS) nanowires on Si(111).

2. Experiments
InGaAs/GaSb CS NWs were grown on Si by selective-area MOVPE. First, a 20-nm-thick SiO_2 film was formed Si(111) by thermal oxidation. Periodical mask openings were formed using electron beam lithography, dry and wet etchings. Next, InGaAs NWs were grown. Details for integrating vertical InGaAs NWs on Si(111) were the same as previous reports [2]. Trimethylindium (TMIn), trisdimethylaminoantimony (TDMASb), arsine (AsH_3), trimethylgallium (TMGa) were used as source materials. Diethylzinc (DEZn), monosilane (SiH_4) were used as dopant sources. Si-doped InGaAs NWs were grown for 15 min. The In content in solid phase was 70%. Next, Zn-doped p-GaSb layers were grown at 480°C - 540°C for 5 and 10 min. The partial pressure of TMGa and TDMASb were 2×10^{-6} atm and 2×10^{-4} atm, respectively. The carrier concentration of the Si doping layer and Zn-pulse-doped layer were of the order of 1×10^{-17} cm^{-3} and 1×10^{-19} cm^{-3}, respectively.

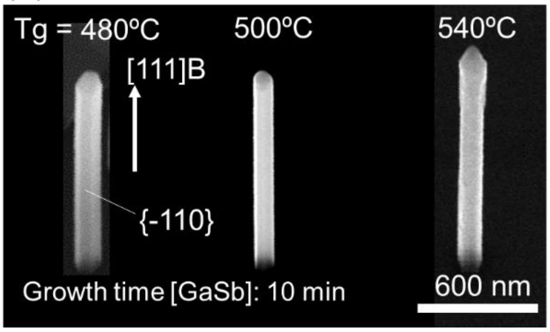
As for vertical diode devices, first, 5-nm-thick Al_2O_3 was formed on NWs as protection layer by atomic layer deposition. Next, NWs were covered with benzocyclobutene (BCB) formed by spin-coating and then metal contact region was exposed by reactive ion etching (RIE) removing BCB on the top portion of the NWs. Next, Al_2O_3 of metal contact area were etched. Then, Ti/Au and Ni/Au were evaporated on the top of the NWs and bottom side of the substrate, respectively. Finally, the samples were annealed at 350°C in N_2.

3. Results and discussions
The InGaAs/GaSb CS NWs grown on Si is shown in Fig.1(a). The NWs were vertically aligned on Si(111). The X-ray diffraction ω-2θ scans of InGaAs/GaSb CS NW array with various distance between NWs in Fig.1(b) showed peak at 25.9 degrees, indicating that the GaSb shell were grown.

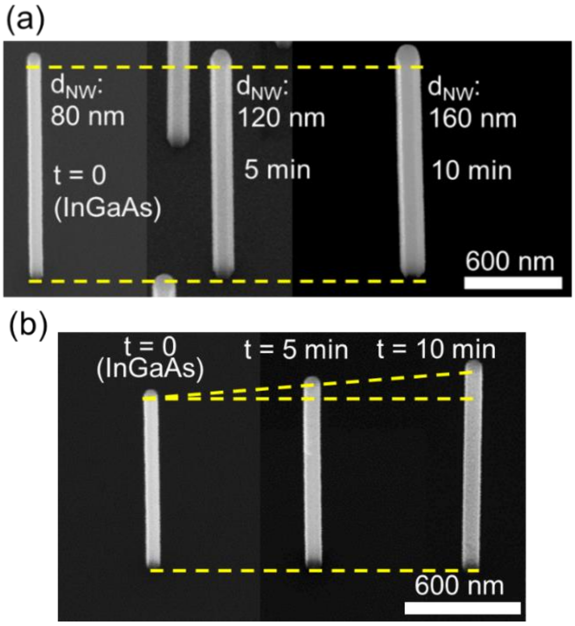
We compared InGaAs/GaSb CS NWs at different growth temperature of GaSb shell which is shown in Fig. 2. At the growth temperature (T_g) = 480°C, the GaSb layer was grown



Figures 1. (a) 30°-tilted view SEM image of InGaAs/GaSb CS NW array on a Si(111) substrate. (b) XRD profile of InGaAs/GaSb CS NWs on Si(111) substrate.



Figures 2. SEM image showing InGaAs/GaSb CS NWs at different T_g of GaSb.



Figures 3. SEM images of the InGaAs/GaSb CS NWs at different growth times of GaSb: (a) T_g = 480°C, (b) T_g = 500°C.

along <-110> directions, and the axial growth along [111]B direction was suppressed. The vertical {-110} sidewalls maintained smooth surface, indicating that the GaSb shell was uniformly grown on the InGaAs NWs sidewalls. At T_g = 500°C, the GaSb were grown on the top facet of the NWs, indicating 2D GaSb islands were coalesced. At T_g = 540°C, GaSb was grown preferentially in axial [111]B direction. And, GaSb were grown on the sidewalls of the NW partly. Thus, surface morphology for the GaSb roughened at T_g > 500°C. This is because incorporation and absorption processes of Sb atoms on the NWs sidewalls and top (111)B surface is competed due to high growth temperature, resulting in the inhomogeneity of the coverage of Sb adatoms.

Figures 3(a) and (b) exhibit growth time dependence for the InGaAs/GaSb CS NWs at T_g =480°C and 500°C. At T_g = 480°C, the diameter of NWs was increased as the growth time, while the NW height was almost constant. This indicated that the lateral-over growth (LOG) was proceed with a growth rate ~2 nm/min. At T_g = 500°C, the NW-height was linearly increased as the growth time, and the LOG slightly occurred. On the other hand, the LOG was nonlinearly increased. Thus, we revealed that optimum T_g for GaSb shell layer was ~480°C.

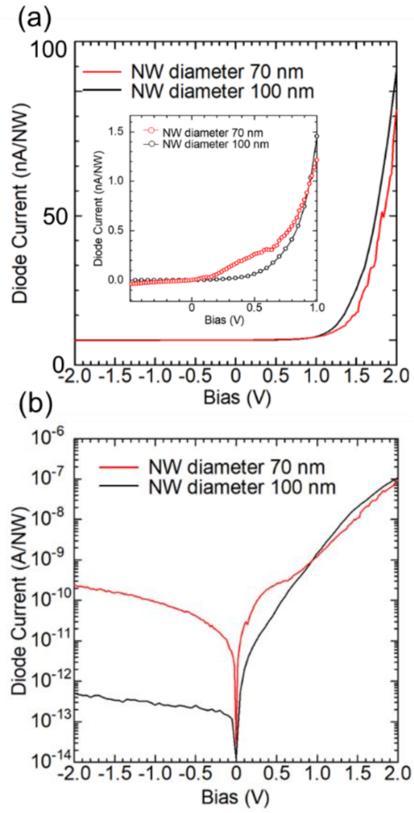


Figure 4. Current-voltage characteristics of two-terminal device with n-InGaAs p-GaSb core-shell NW with different core diameter. (a) Linear plot, (b) Semilogarithmic plot.

The current-voltage (I-V) characteristics are shown in Figs. 4(a) and (b). The two-terminal devices were compared at different NW diameters (70 nm and 100 nm). In this device configuration, n-Si substrates were grounded. The both devices showed good rectifying properties. The device with NW diameter of 70 nm exhibited negative differential resistance at forward bias of +0.4 V. This indicates that n-InGaAs NW/p-GaSb shell heterointerface can induce band-to-band tunneling transport. Ideality factor was ~3.3. The large ideality factor was originated from high contact resistance. The detailed crystal structure and electrical properties of the CS NW will be discussed.

4. Conclusions

We have demonstrated integration of InGaAs/GaSb CS NWs on Si(111) by selective-area growth and the NW vertical diodes. The lateral growth of GaSb shell layer was dominant at T_g = 480°C. At T_g > 500°C, the axial and radial growth of GaSb competed. The device with NW diameter of 70 nm showed good rectifying properties with negative differential resistance.

Acknowledgements

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