Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp573-574

The demonstration of *SS* below 60 mV/dec at RT in all 2D heterostructure TFET

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Abstract: Van der Waals heterostructures are the ideal material platform for tunnel field effect transistors (TFETs) because a band-to-band tunneling (BTBT) dominant current is feasible at room temperature (RT) due to ideal, dangling bond free heterointerfaces. However, achieving subthreshold swing (SS) values lower than 60 mVdec^{-1} of the Boltzmann limit is still challenging. In this work, we demonstrate all 2D type III *n*-MoS$_2$/*p*$^+$-MoS$_2$ heterostructure TFETs with SS values less than 60 mVdec^{-1} at RT.

1. Introduction

For the 2D/2D interfacial properties in TFET, the defect-free clean heterointerface is critical for obtaining the BTBT dominant current under reverse bias at the diode. Although the BTBT current has been demonstrated at low temperatures, thermally activated behavior often appears at higher temperatures near RT. That is, the generation current governs the total current, resulting in degradation of the SS at RT. This suggests that interface states exist even for 2D/2D interfaces. In general, high-*k* top gate oxides have been used in most of 2D TFETs reported thus far to enhance the gate capacitance. However, how the quality of the 2D/2D interface is affected by the deposition of high-*k* oxides has not been revealed yet. Therefore, comparisons between high-*k* and *h*-BN gate insulators should be carried out systematically in the same 2D TFET system, because the use of *h*-BN in TFETs has been quite limited.

In this work, we systematically studied all 2D heterostructure TFETs produced by combining the type III *n*-MoS$_2$/*p*$^+$-MoS$_2$ heterostructure with the *h*-BN top gate in order to achieve SS values less than 60 mVdec^{-1} at RT.

3. Strategy in 2D/2D TFET structure

There are three strategies to further reduce the SS values: (i) Recently, we have discovered that the deposition of Al_2O_3 top gate oxide on the MoS_2 channel increases the interface states density due to the introduction of strain in the MoS_2 channel on the *h*-BN substrate.[1] Therefore, an *h*-BN top gate insulator was adopted to benefit from the electrically inert interface in 2D heterostructure TFETs. (ii) The *p*$^+$-MoS$_2$ source was used because the E_F of *p*$^+$-MoS$_2$ cannot be modulated due to the degenerately high doping of the *p*$^+$-MoS$_2$. (iii) According to the transmission probability calculated for carrier transport through the BTBT barrier,[2] the E_G for the channel should be larger than that for the source to keep the off current low but E_G also should be as small as possible to increase the transmission probability. Therefore, the 1L and 3L MoS_2 channels were compared. Based on these three considerations, all 2D heterostructure TFETs were fabricated to achieve SS values lower than 60 mVdec^{-1}.

3. Results and Discussion

Figure 1 shows a schematic (a) and an optical micrograph (b) of a typical *h*-BN/*n*-MoS$_2$/*p*$^+$-MoS$_2$/*h*-BN all 2D heterostructure TFET. The typical thickness for the top gate *h*-BN insulator and the *p*$^+$-MoS$_2$ source are ~15 nm and ~30 nm, respectively. The atomically sharp gate stack interfaces are clearly seen in the cross-sectional TEM image of **Figure 1c** since all of the 2D materials are stable in air. As was expected, the diode properties of the all 2D heterostructure TFET with the 3L-*n*-MoS$_2$ channel in **Figure 2a** shows the type III band alignment at V_{TG} = 6 V. The negative differential resistance (NDR) trend at the forward side is not visible. This could be explained by the

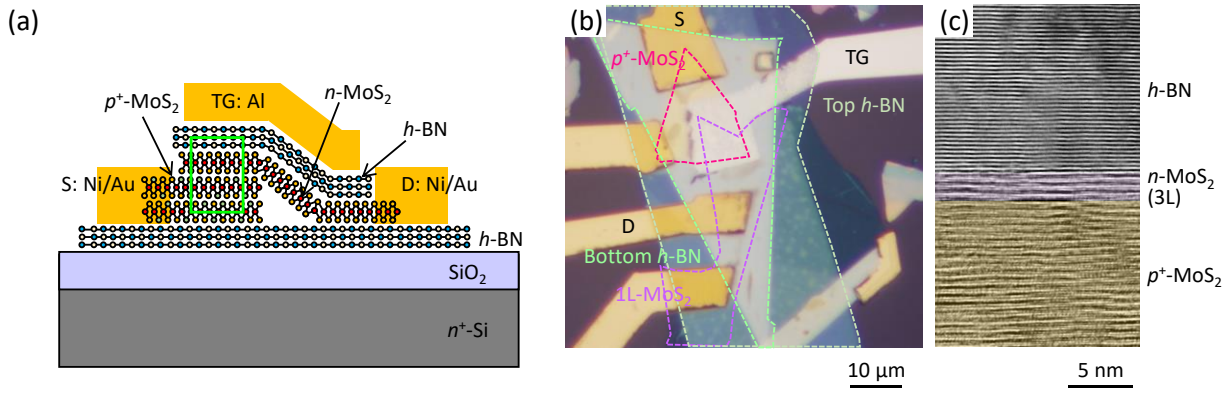

Figure 1 a) Schematic illustration and b) optical micrograph of all 2D heterostructure TFET. c) Cross sectional TEM image of all 2D heterostructure at the solid rectangular in a). The number of MoS_2 layers is 3.

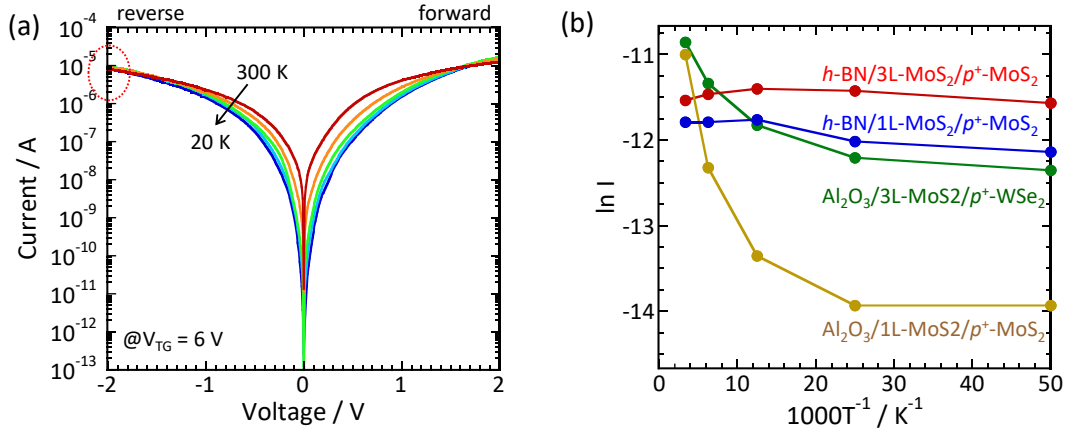

Figure 2 a) Diode properties in the 3L-*n*-MoS_2/p^+-WSe_2 heterostructure at V_{TG} = 6 V and different temperatures (20, 40, 80, 160, and 300 K). b) Arrhenius plot of the current at the reverse bias of -2 V for different heterostructures.

barrier between the conduction band minimum for p^+-MoS_2 and the valence band maximum for the *n*-MoS_2 channel because the E_G of bulk MoS_2 (~1.4 eV) is larger than the E_G of bulk WSe_2 (~1.2 eV). An Arrhenius plot of the current at the reverse bias of -2 V is compared with other heterostructures in **Figure 2b**. It should be noted that all four heterostructure TFETs exhibit type III band alignment. For the *h*-BN top gate heterostructure devices with the 1L and 3L MoS_2 channels, temperature-independent behavior is evident over the entire temperature range, indicating that BTBT is dominant even at RT. This is quite promising for TFET operation with low SS values at RT. On the other hand, when Al_2O_3 was used as the top gate insulator, thermally activated behavior at high temperatures was clearly observed regardless of the source crystal. These comparisons indicate that the trap-related generation-recombination current [3] and/or the trap-assisted tunneling current under reverse bias are drastically suppressed by the successful integration of the electrically inert interface in the 2D heterostructure TFET.

Finally, the transfer characteristics of the 2D heterostructure TFETs at the reverse bias of -2 V at RT are shown in **Figure 3a**. The estimated SS values are shown as a function of ID in **Figure 3b**. For the 3L-*n*-MoS_2 Boltzmann limit was achieved at RT. Since the *SS* value for the 1L-*n*-MoS_2 channel was over 100 mV/dec, the smaller E_G of the 3L-*n*-MoS_2 channel was preferable. However, leakage current contributions should be considered carefully since artificially low SS values are often reported. We have confirmed that I_D overlaps with I_S for the 3L-*n*-MoS_2 channel because there is no gate leakage, which supports that the *SS* value is lower than 60 $mVdec^{-1}$ at RT.

4. Conclusion

The key finding regarding the quality of the heterointerface is that producing the defect-free clean heterointerface via integration of the *h*-BN top gate provides the BTBT dominant current even at RT. All 2D heterostructure TFETs produced by combining the type III *n*-MoS_2/p^+-MoS_2 heterostructure with the *h*-BN top gate insulator resulted in SS values less than 60 $mVdec^{-1}$ at RT.

Acknowledgements: This research was partly supported by the JSPS Core-to-Core Program, A. Advanced Research Networks.

References: [1] N. Fang, S. *et al.*, Adv. Func. Mater. 2019, 29, 1904465. [2] A. M. Ionescu, *et al.*, Nature 2011, 479, 329. [3] T. Gotow, *et al.*, J. Appl. Phys. 2019, 126, 214502.

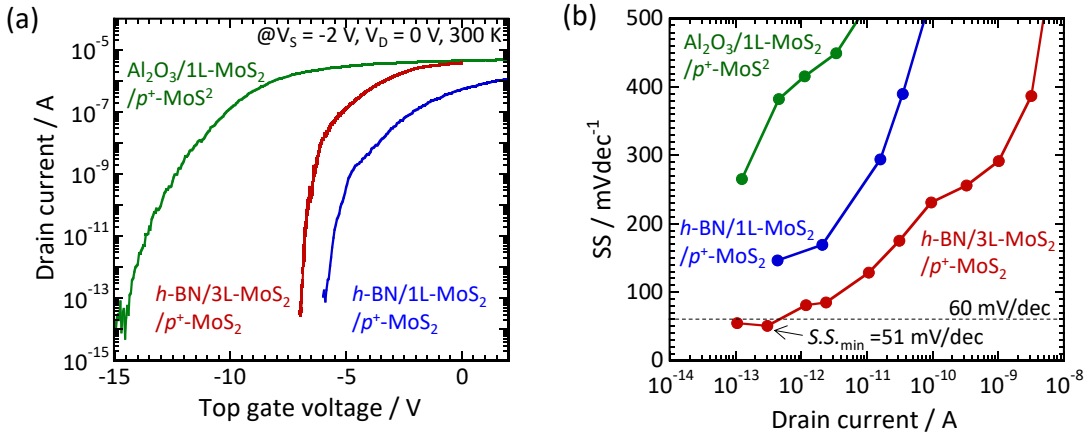

Figure 1 a) Transfer characteristics for the three different heterostructure TFETs. b) SS as a function of I_D for the three different heterostructure TFETs.