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TiN/MgO/Si memristive devices as a selectorless synapse for ultralow-power analog neuron chip and time-series applications

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Abstract

Memristive devices have been attracting attention as synapse devices for neuromorphic hardware. A selectorless memristive device with variable resistance and a diode effect is promising for further power reduction of fast analog neuron chips. Such devices are also expected to recognize time-series data by means of recurrent data processing in their array. In this work, we developed a TiN/MgO/Si CMOS-compatible memristive device and demonstrated experimental readouts and time-series data processing on the arrays made for a kilo-bit-class configuration.

1. Introduction

Driven by the recent advances with deep learning, artificial intelligence (AI) and neural network (NN) technologies have been increasingly studied [1]. Since NNs are made up of signal processing and algorithms that model the human brain, the low-power hardware they use has been developed taking a neuromorphic approach [2]. In NN learning, synaptic weights, which are the element of memory, are updated repeatedly. Due to the time- and energy-consuming nature of the learning process, energy-efficient architectures for emerging devices is now required, especially for synapse devices [Marukame]. One promising synapse device is a memristor or memristive device [3, 4]. By configuring the memristor in an array of crossbars or cross-points, NN's sum-of-products operator can be integrated at high density [3]. Spike-timing dependent plasticity (STDP) that mimics brain plasticity has been investigated in TiN/MgO/WO_x devices [5]. Recently, a highly efficient multiplier accumulator and vector matrix multiplier composed of ferroelectric tunnel junction (FTJ) memristors was proposed [6]. As the current-voltage (*I-V*) characteristics of FTJs are quite asymmetric due to their energy potential structure, they are used as the selectorless resistive device in a crossbar. The memristive properties of HfO_x-based ferroelectricity and the high reliability of these memristive devices makes them promising as CMOS-compatible memory devices.

Various Metal/Insulator/Si (MIS) structures have been explored over the last few decades of the CMOS scaling era. One of these is the high-*k* metal gate structure, examples of which include, TiN/MgO/Si and TiN/$HfSiO_x$/Si [7]. In the present study, we focus on this structure as a tunnel device and have developed a TiN/MgO/Si memristive device in order to achieve a diode effect. In addition, we recently demonstrated low-power stable and fast neuron circuits using variable resistors as a synapse [5], and in the present study, we discuss the network configurations of our developed memristive arrays and various operation sequences to explore new applications.

2. TiN/MgO/Si memristive devices as a synapse

We adapted our previously reported TiN/MgO/WO_x [5] to include a lower electrode, as shown in Fig. 1(a). A thin MgO film was deposited on the Si substrate to form a tunnel junction using a fabrication technique developed in the past for spin-MOSFET electrodes [8]. The crystal structure of MgO can be controlled by a condition of the Si surface, clean or unclean, and by MgO deposition conditions through electron beam evaporation. The first interlayer (IL1) between Si and MgO and the IL2 between MgO and TiN were formed. SiO_x for IL1 was formed inherently on an uncleansed Si substrate, and Mg was intentionally inserted into the films to change the device structure. Figure 1(b) shows the typical *I-V* characteristics with an obvious diode effect in the TiN/MgO/(SiO_x)/Si. Figure 1(c) shows similar curves, however, the current rises rapidly after the break-down on the positive voltage side. It seems that the break-down, i.e., forming process, enables a 10× higher current than in (b) while maintaining the plasticity.

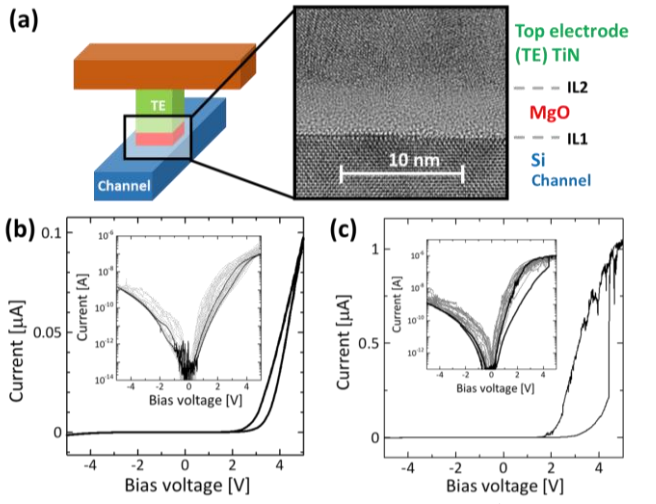

Fig. 1 TiN/MgO/Si memristive device. (a) Illustration of the device structure and transmission microscope image of the film stack. (b) Current-voltage (*I-V*) characteristics of the device shown in (a) with IL1 (SiO_x) and without IL2. (c) *I-V* characteristics of the device with IL2 (Mg). Insets of (b) and (c) show log-scale and data taken from many cycles.

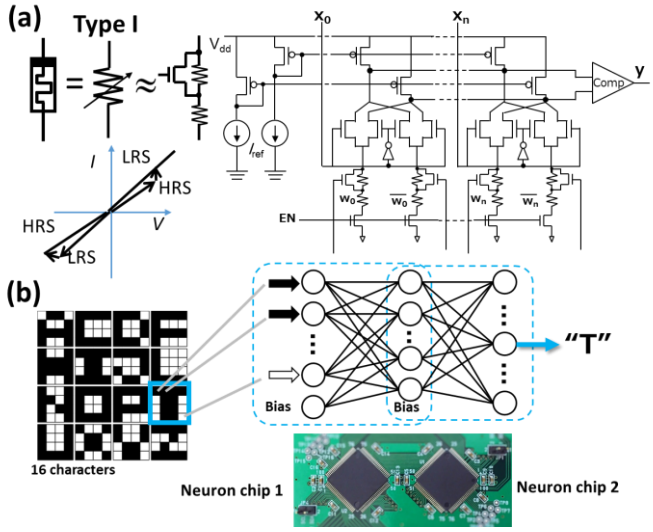

Fig. 2 Memristive device applications for neural network circuits. (a) Memristive device Type I features a variable resistance (both low-resistance state (LRS) and high-resistance state (HRS)) and can also be implemented with poly-silicon and a pass transistor in analog neuron circuits [5]. (b) A pattern matching application with two analog neuron chips that can recognize alphabet character patterns fast (response time: less than approximately 4 μs with ~20 mW).

3. Sequential data processing with analog neuron chips and recurrent network using TiN/MgO/Si devices

Memristors can be categorized into two types: I and II. Type I does not have any diode effects and is used in analog neuron chips (Fig. 2). It is expected to further improve the performance of this type of chip, which has low-power consumption (~20 mW) and a fast response time (less than approximately 4 μs) in a two-chip-series connection. The synapses of the neuron chip can also be composed of poly-silicon resistors and a pass transistor. Since the recognition results are static, in order to use these chips recurrently for time-series processing, it is necessary to have another network configuration. Type II of TiN/MgO/Si was fabricated to make a 32×32 crossbar array (Fig. 3). Although the diode effect enables us to obtain the individual device characteristics by means of pulse-voltage writing, they did not show clear STDP curves possibly due to the strong nonlinearity. Figure 3(c) shows the resistance map of a 1-kbit readout at the standard voltage of 3.3V for a microcontroller. Since the resistances between the devices are different, two Type II devices are used as a pair to form synaptic weights, and the comparator is used to output *y*, as shown in Fig. 4(a). The results of alphabet character recognition in the neuron chip are input to this network, and thus the output is recursively and sequentially processed. The results of simulations and experiments (Fig. 4(b)(c)) demonstrate that it is possible to obtain a state transition map.

4. Conclusion

In this study, we developed a TiN/MgO/Si selectorless memristive device that can be integrated in a crossbar array. By combining the memristive devices with low-power analog neuron chips performing fast pattern recognition, we demonstrated successful time-series data processing in simulations and experimental sequences.

References

[1] G. E. Hinton and R.R. Salakhutdinov, Science **313** (2006) 504.
[2] P. A. Merolla, *et al*., Science **345** (2014) 668.
[3] M. Prezioso, *et al*., Nature **521** (2015) 61.
[4] T. Marukame, *et al*., IEEE TCAS2: Express Briefs. **64** (2016) 462.
[5] T. Marukame, *et al*., Jpn. J. Appl. Phys. **59** (2020) 040606.
[6] R. Berdan, T. Marukame, *et al*., Nature Electronics **3** (2020) 259.
[7] N. Mise, *et al*., IEDM (2007) 527.
[8] T. Marukame, *et al*, IEDM (2009) 215.

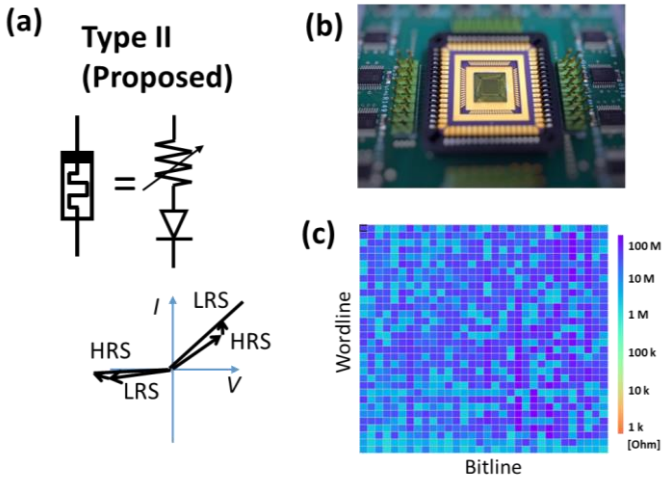

Fig. 3 Devices for integration. (a) Type II memristive devices (TiN/MgO/Si) feature a variable resistance with a diode effect. (b) A photo of the chip that contains 32×32 (1-kbit class) devices. (c) Initial read of all 1-kbit devices at 3.3 V (synapse map).

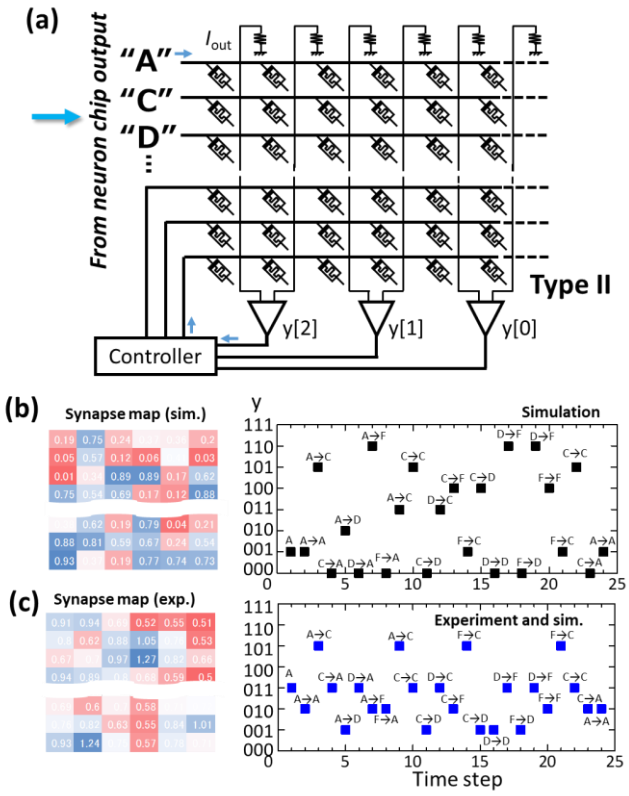

Fig. 4 Example of recurrent and sequential neural network application. (a) Network organization consisting of Type II memristive devices. This can be stimulated by the neuron chip after its pattern recognition. The controller receives the output signal from comparators and passes them for its own reoccurrence. (b) Simulations of recurrent output generated with input of sequential A, C, D, and F based on randomized memristive values. (c) Experimental results with fabricated TiN/MgO/Si devices and a microcontroller.