# High Hole-mobility (690 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>) Flexible Polycrystalline Ge Thin Films

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## Abstract

Polycrystalline Ge layers are fabricated on a plastic substrate using low-temperature (500 °C) solid-phase crystallization of densified amorphous precursor. The 400-nm-thick Ge layer exhibited the Hall hole mobility of 690 cm<sup>2</sup>/Vs, exceeding that of single-crystal Si wafers.

## 1. Introduction

Ge on insulator (GOI) technology has been widely studied for lowering the fabrication cost and improving the device performance of Ge metal-oxide-semiconductor fieldeffect-transistors. Solid-phase crystallization (SPC) is a simple method to directly form polycrystalline Ge (poly-Ge) thin films on glass substrates at low temperatures [1]. We recently advanced conventional SPC method and achieve the large grain Ge thin film with high hole mobility [2,3]. In addition, by applying thin film transistor (TFT), demonstrated excellent p-channel TFT characteristics [4]. In this study, to achieve both flexibility and higher TFT performance, we develop this SPC-method onto plastic substrate, and realize flexible Ge thin film with highest hole mobility 690 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>.

## 2. Experimental Procedures

In the experiment, 50-nm-thick insulating underlayer (SiN, Al<sub>2</sub>O<sub>3</sub>, GeO<sub>x</sub>) was formed on both SiO<sub>2</sub> glass and plastic (Polyimide) substrates by RF magnetron sputtering. After that, amorphous Ge (a-Ge) layer was deposited by vacuum deposition while heating at 150 °C. The film thickness of the a-Ge layer ranged from 100 to 500 nm. The samples were then loaded into a conventional tube furnace in an N<sub>2</sub> atmosphere annealed at 375-450 °C for 5-150 h to induce SPC. After annealing for SPC, the grown Ge layers were evaluated by using electron backscattering diffraction (EBSD) analysis, Raman spectroscopy and analytical transmission electron microscope (TEM). The electrical properties of the SPC-Ge layers were evaluated using Hall effect measurements.

## 3. Results and Discussion

EBSD images in Figs. 1(a)–1(d) show that the grain size of the SPC-Ge layer strongly depends on the kind of the underlayer. This suggests that the frequency of Ge nucleation was changed because of the change of the interfacial energy between Ge and the underlayer. From the EBSD analyses, the average grain size was determined to be 2.9  $\mu$ m for SiO<sub>2</sub>, 1.4  $\mu$ m for SiN, 5.3  $\mu$ m for Al<sub>2</sub>O<sub>3</sub>, and 4.5  $\mu$ m for GeO<sub>x</sub>. All samples showed p-type conduction, similar to conventional undoped SPC-Ge on glass. This is because the point defects in Ge provide shallow acceptor levels that generate holes at room temperature. Figure 1(e) shows that the hole concentration *p* and the hole mobility  $\mu$  also depend on the underlayer material. The GeO<sub>x</sub> sample exhibits the lowest *p* and the highest  $\mu$  among these underlayer materials. This improvement of  $\mu$  likely reflects the reduction of grain boundary scattering and impurity scattering. Therefore, we examined further improvement of carrier mobility focusing on the GeO<sub>x</sub> sample.

The Raman spectra in Fig. 2(a) show the broad peaks corresponding to a-Ge before annealing and the sharp peaks corresponding to crystalline Ge (c-Ge) after annealing [2]. The wavenumber of the c-Ge peak of each SPC-Ge shifts in the opposite direction from that of bulk-Ge. Figure 2(b) shows that, for all t, the c-Ge peak in glass samples shifts to a lower wavenumber, while that in plastic samples shifts to a higher wavenumber from that of bulk-Ge. According to the Raman shifts and the equation proposed by Chen et al., [5] the tensile strain in the glass sample is approximately 0.48% and the compressive strain in the plastic sample 0.70%. The cause of the strains can be explained from the perspective of the thermal expansion difference between the substrate and Ge. Considering the relationship of these thermal expansion coefficients, tensile strain is applied to Ge on glass while compressive strain is applied to Ge on plastic during the cooling process



Fig.1 (a)-(d) EBSD images of the 300 nm thick Ge layers with various underlayers. (e) Underlayer dependence of electrical properties.



Fig.2 (a) Raman spectra of the samples before and after annealing. (b) Peak shifts from Ge substrate and (c) FWHMs of the Ge-Ge peaks as a function of t.

after Ge crystallization. Figure 2(c) shows that the full width at half maximum (FWHM) of the c-Ge peak is almost constant with respect to t, while the plastic samples exhibit lower FWHMs than the glass samples for all t. This behavior indicates that the plastic samples have higher crystallinity than the glass samples.

We evaluated the electrical properties of the samples. As shown in Fig. 3(a), p is almost constant with respect to t, while  $\mu$  increases with increasing t [3,7]. Both p and  $\mu$  have no significant differences between glass and plastic samples. We estimated GB barrier height  $E_{\rm B}$  by the conduction model in polycrystalline semiconductors proposed by Seto [6]. As shown in the inset in Fig. 3(b), it is found that the influence of grain boundary scattering differs depending on t. In addition, the shapes of the Arrhenius plots significantly differ between glass and plastic samples, indicating a large difference of  $E_{\rm B}$ . Figure 3(b) shows that  $E_{\rm B}$  decreases with increasing t. Especially for t = 100 nm,  $E_{\rm B}$ shows high values, suggesting that the GB property near the  $Ge/GeO_x$  interface is inferior. We note that the plastic sample exhibits a lower  $E_{\rm B}$  than that of the glass sample for all t. The  $E_{\rm B}$  difference is explained from the perspective of strain (Fig. 1). For the glass sample, Ge has in-plane tensile strain, which likely increases dangling bonds (i.e., trap density) in the GBs, increasing  $E_{\rm B}$ . In contrast, for the plastic sample, Ge has in-plane compressive strain, which promotes Ge bonding in the GBs, decreasing  $E_{\rm B}$ .

To evaluate the detailed cross-sectional structure for the sample on plastic, we used TEM analysis. Figure 4(a) and (b) show that a flat-surface Ge layer is formed on plastic substrate and the stacked structure of Ge/GeO<sub>x</sub>/plastic as intended. Figure 4(c) shows that the atomic ratio of Ge and O in the GeO<sub>x</sub> layer is 2:3. Figure 4(d) shows there are no extended defects in the vicinity of the Ge/GeO<sub>x</sub> interface. Figure 4(e) shows that the interface between Ge and GeO<sub>x</sub> is rough, suggesting that it causes  $\mu$  degradation for  $t \leq$  300 nm. In addition, the Ge crystals region are included in the GeO<sub>x</sub> layer, indicating the desorption of oxygen during the crystallization process.

For further improvement, we have performed Post annealing (PA; 500 °C, 5 h) for the Ge film (400 nm) on high heat-resistant plastic. Figure 5(a) shows that the  $\mu$  values are maintained around a bend angle of 50°, while decreases significantly when the bend angle exceeds approximately 50°. The decrease in  $\mu$  is due to the occurrence of cracks in the film. The results obtained in this research are summarized in Fig. 5(b). After PA, impurity scattering was suppressed by reducing the defect-induced acceptors and the hole mobility was dramatically improved (500  $\rightarrow$  690 cm<sup>2</sup>  $V^{-1}$  s<sup>-1</sup>). This value is higher than that of Ge on the glass substrate [3], and is the highest among all the low-temperature films synthesized on insulator substrates. It is also attractive because it surpasses that of a single-crystal Si wafer [8]. These results mean that single-crystal wafers are no longer necessary for fabricating semiconductor films with a high carrier mobility.

## 4. Conclusion

We realize to develop high quality SPC-Ge layer onto plastic by controlling *t* (100–500 nm) and inserting GeO<sub>x</sub> underlayer (50 nm) and PA. The resulting hole mobility 690 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> is the highest value to date among all the

low-temperature films synthesized on insulator substrates. This achievement will give a way to realize advanced electronic and optical devices simultaneously allowing for high performance, inexpensiveness, and flexibility.

#### References

- [1] K. Toko et al., Solid-State Electron. 53, 1159 (2009).
- [2] K. Toko et al., Sci. Rep. 7:16981 (2017).
- [3] T. Imajo et al., Appl. Phys. Express. 12, 015508 (2019).
- [4] K. Moto et al., Appl. Phys. Lett. 114, 2107 (2019).
- [5] H. Chen et al., Phys. Rev. B 65. 233303 (2002).
- [6] J. Y. W. Seto, J. Appl. Phys. 46, 5247 (1975).
- [7] R. Yoshimine et al., Appl. Phys. Express. 11, 031302 (2018).
- [8] J. C. Irvin & S. M. Sze, Solid-State Electron. 11, 599 (1968).
- [9] N. Hirashita et al., Appl. Phys. Express. 1, 1014011 (2008).
- [10] W. Takeuchi et al., Appl. Phys. Lett. 107, 022103 (2015).

[11] J. -H. Park et al., Appl. Phys. Lett. 104, 252110 (2014).



Fig.3 (a) p and  $\mu$  as a function of t. (b)  $E_{\rm B}$  as a function of t. Inset shows representative Arrhenius plots of  $\mu T^{1/2}$  for t = 100 nm and 400 nm.



Fig.4 Characterization of the cross-section of the sample for Ge layer grown on plastic substrate after PA. (a) HAADF-STEM image. (b) EDX elemental mapping. (c) EDX depth profile along the arrowed line in (a). (d) Bright-field TEM image. (e) High-resolution lattice images showing the  $Ge/GeO_x$  interface.



Fig.5 (a)  $\mu$  as a function of bend angle for t = 100 nm and 400 nm. (b) Comparison of  $\mu$  and p of Ge films on insulators.