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High Carrier Mobility of Sn-Doped Ge Thin-Films (~20 nm) on Insulator by Interface-Modulated Solid-Phase Crystallization

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Abstract

Electrical properties of Sn-doped Ge films (thickness ≤50 nm) on insulator obtained by interface-modulated solid-phase crystallization have been investigated. The carrier mobilities of grown films significantly decrease with decreasing thickness. which are caused by decrease in the grain sizes and increase in the energy barrier heights at grain boundaries. To improve carrier mobility of thin films, we propose thinning of grown films (deposition thickness: 50 nm) by etching. This enables formation of Sn-doped Ge thin-films (thickness: 20 nm) with high carrier mobility (~170 cm^2/Vs). This mobility is the highest among ever reported data for Ge and GeSn thin-films (thickness: ≤30 nm) on insulator grown at low-temperature (450ºC).

1. Introduction

Low-temperature (≤500ºC) formation of fully-depleted thin-film transistors (TFTs) with high-speed operation and low-power consumption is required for next-generation electronics, such as three-dimensional large-scale integrated circuits and advanced system-in-displays [1]. For this purpose, high-carrier-mobility semiconductor thin-films (thickness: ≤20 nm) on insulator structures should be fabricated under low-temperature processing conditions (≤500 °C).

Previously, we investigated interface-modulated solid-phase crystallization (SPC) of Sn-doped a-Ge films (thickness: 50 nm) [2]. By introduction of a-Si thin under-layers between Sn-doped Ge and insulating substrates, interface nucleation in Sn-doped Ge films is suppressed, and high carrier mobility of ~300 cm^2/Vs was obtained [2]. However, Ge films with smaller thickness below 20 nm are required for application to advanced TFTs with short channel length.

In the present study, thickness-dependence of electrical properties of Sn-doped Ge films with thicknesses below 50 nm are investigated. Based on the results, a technique to obtain Ge thin-films (thickness: ~20 nm) with high carrier mobility is developed.

2. Experiments and Results

In the experiment, a-Si (thickness: 5 nm) and a-GeSn layers (Sn concentration: 2%, thickness: 20-50 nm) were deposited on fused-quartz substrates using a molecular-beam deposition system (base pressure: ~5×10^{-10} Torr). The sample structure is schematically shown in Fig. 1. The samples were annealed at 450℃ for 20-40 h to induce SPC.

Electrical properties and grain structures of grown Ge layers were analyzed by Hall effect and electron backscattering diffraction (EBSD) measurements.

The carrier mobility of samples (deposition thickness: 30 and 50 nm) are shown by blue symbols in Fig. 1, as a function of the thickness, which shows that the carrier mobilities decrease with decreasing thickness. It is noted that the mobility of the sample with deposition thickness of 20 nm could not be measured, because the sample resistance was very high. The grain sizes of the samples, obtained by EBSD, are shown by blue symbols in Fig. 2, as a function of the thickness. This figure shows that the grain sizes significantly decrease with decreasing deposition thickness.

These results suggest that the decrease in the carrier mobility with decreasing deposition thickness should be caused by decrease in the grain sizes. Thus, it is expected that high carrier mobility will be obtained by enlargement of grain sizes even for thin-films (thickness: ≤50 nm). This triggers an idea of thinning of grown Ge films (deposition thickness: 50 nm), consisting of large grains.

To examine this idea, we performed etching of grown Ge films (deposition thickness: 50 nm) and measured carrier mobilities and grain sizes. The results are shown by red symbols in Figs. 1 and 2. As expected, the thinned samples keep large grains as shown in Fig. 2. On the other hand, Fig. 1 shows that the carrier mobilities still decrease with decreasing thickness after thinning, though the mobilities become larger compared with the sample (deposition thickness: 30 nm) without thinning, and mobility of ~170 cm^2/Vs is obtained for thickness of 20 nm.

To reveal the phenomena, we analyzed grain boundaries using Seto's model [3]. Figure 3 shows Arrhenius plot of $\mu T^{1/2}$ for the films with and without thinning, where μ is the mobility and T the absolute temperature. Respective data are well fitted with straight lines. From the slopes of these lines, energy barrier height E_B at grain boundaries is evaluated, which is summarized as a function of the thickness in Fig. 4. E_B is ~5 meV for the sample (deposition thickness: 50 nm) without thinning and increase to ~7 meV for the sample (deposition thickness: 30 nm), which shows a good agreement with the decrease in the carrier mobilities as shown in Fig. 1. On the other hand, E_B is as small as ~5 meV for the sample (deposition thickness: 50 nm) after thinning to 30 nm. Thus, the decrease in the mobility after thinning can not be explained on the basis of change in E_B. Possible reason for the decrease of the mobilities is carrier scattering at the interface and surface of the Ge films. Further investigation is required to reveal the detail.

Figure 5 shows mobility obtained in the present study, comparing with literature data for Ge and Sn-doped Ge (GeSn) on insulator grown at low temperatures (≤500°C) [2,4-7] as a function of the film thickness. Thin films (≤20 nm) are required to realize advanced fully-depleted devices with short channel length. Figure 5 shows that the present technique provides the highest mobility among ever reported data of thin films.

3. Conclusion

In summary, we have developed a technique to realize high carrier mobilities of Ge thin films on insulator. By low-temperature annealing (450°C) of a-GeSn films having a-Si thin under-layers and subsequent thinning, poly-crystalline Sn-doped Ge films having large grains (~2 μm) are obtained. As a result, high carrier mobility of ~170 cm^2/Vs is obtained for thickness of 20 nm, which is the highest among ever reported data of Ge and GeSn on insulator grown at low-temperatures (≤500°C). This technique will facilitate advanced fully-depleted devices for next-generation electronics.

References

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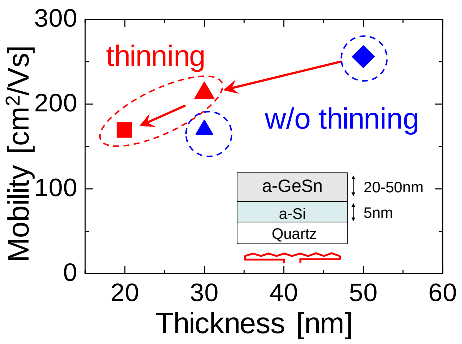

Fig.1. Initial sample structure and thickness dependence of carrier mobility for samples without thinning (▲,◆) and after thinning of 50-nm-thick grown films (■,▲).

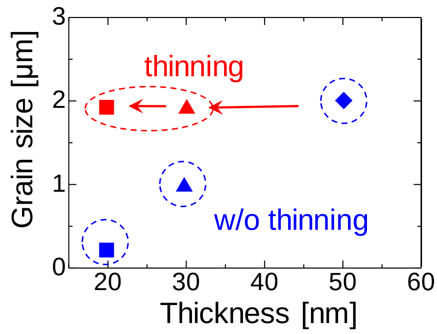

Fig.2. Thickness dependence of grain size for samples without thinning (■,▲,◆) and after thinning of 50-nm-thick grown films (■,▲).

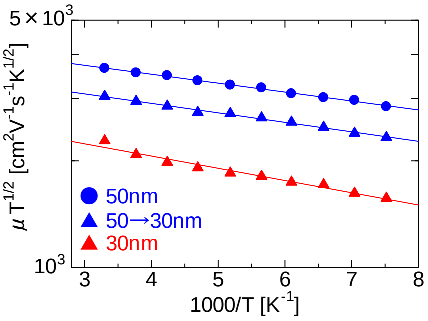

Fig.3. Arrhenius plot of $\mu T^{1/2}$ for samples without thinning (▲,◆) and after thinning of 50-nm-thick grown film (▲).

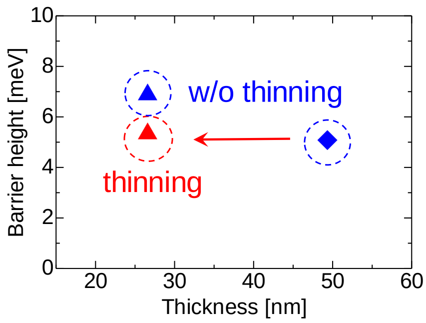

Fig.4. Thickness dependence of the energy barrier for samples without thinning (▲,◆) and after thinning of 50-nm-thick grown film (▲).

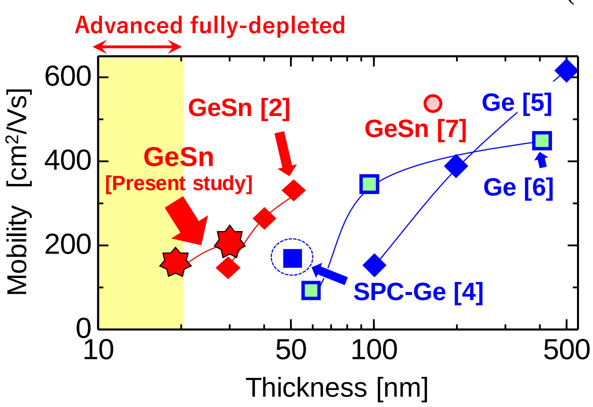

Fig.5. Mobility obtained in the present study compared with those reported for SPC of pure a-Ge [4-6] and a-GeSn [2, 7].