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Gate Stack Technology for Advanced GaN-based MOS Devices

Heiji Watanabe, Takuji Hosoi, Mikito Nozaki, Hidetoshi Mizobata, and Takayoshi Shimura

Graduate School of Engineering, Osaka University
2-1 Yamadaoka, Suita, Osaka 565-0871, Japan
Phone: +81-6-6879-7280 E-mail: watanabe@prec.eng.osaka-u.ac.jp

Abstract

Recent progresses in gate stack technologies for GaN-based MOS devices are introduced from the aspects of material science and interface engineering of the stacks. Superior properties of AlON dielectrics for AlGaN/GaN MOS-HFETs were demonstrated. Thermal oxidation of GaN surfaces was also examined to design insulator/GaN interfaces. Based on the knowledge, high-quality and highly reliable $SiO_2/GaO_x/GaN$ stacked gate dielectrics were proposed.

1. Introduction

Recently, GaN-based power devices have gained much attention for their applications in the next-generation high-frequency and high-power devices. The AlGaN/GaN hetero-junction filed-effect transistors (HFETs) with Schottky gates have been implemented in modern wireless communication. But, their applications are restricted due to the large leakage current through the Schottky contacts and their normally-on operation. To overcome these limitations, MOS gate stacks on GaN-based semiconductors have been studied. Moreover, normally-off vertical power MOSFETs on free-standing GaN substrates have become a hot topic in power electronics.

In contrast with Si-based semiconductors, deposition of wide bandgap insulators on AlGaN and GaN surfaces is thought to be a plausible method for fabricating MOS gate stacks. Among various insulating materials, Al_2O_3 and SiO_2 exhibit a sufficiently wide bandgap and thermal stability for MOS device applications. However, it is well known that Al_2O_3 involves an essential problem of electron trapping, thus leading to significant I_d-V_g hysteresis and V_{th} instability of MOSFETs. In addition, GaN-based MOS devices have much room for improvement in terms of the interface quality and reliability. We developed advanced gate stack technologies for GaN-based power devices through systematic physical and electrical characterizations. This paper reviews our recent progresses in the gate stack engineering for achieving high-quality and highly reliable GaN-based MOS structures.

2. AlON Gate Dielectrics for AlGaN/GaN MOS-HFETs

We have implemented AlON gate dielectrics in SiC MOSFETs [1] and AlGaN/GaN MOS-HFETs [2-4]. As shown in Fig. 1(a), *C*-*V* curves taken from $Al_2O_3/SiO_2/SiC$ gate stacks gradually shifted toward the positive direction as accumulation voltage increased. Nitrogen incorporation into Al_2O_3 (AlON) significantly suppressed *C*-*V* shift, indicating improved immunity against electron injection into the oxide and long-term reliability as shown in Fig. 1(b) [1]. The impact of nitrogen incorporation was also validated by recent first-principles calculations [5].

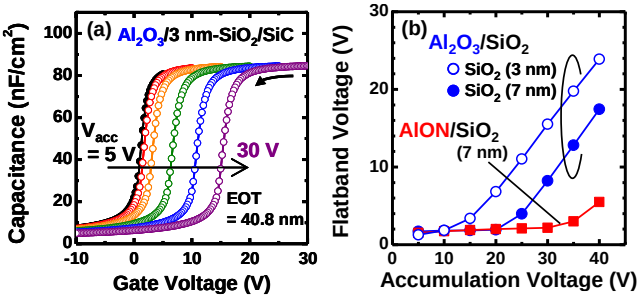

Fig. 1 Typical *C*-*V* characteristics of Al_2O_3/SiO_2 and $AlON/SiO_2$ gate stacks grown on SiC substrates: (a) Positive shift of *C*-*V* curves for Al_2O_3/SiO_2 capacitors. (b) Changes in V_{FB} plotted as a function of maximum accumulation voltage.

Recently, we have applied AlON gate dielectrics to GaN-based power devices. Figure 2 shows a typical TEM image and bidirectional *C*-*V* curves of AlGaN/GaN MOS capacitors [2]. Thanks to the nitrogen incorporation, AlON dielectrics remained amorphous and abrupt AlON/AlGaN interfaces were obtained even after post-deposition annealing at 800°C. Bidirectional *C*-*V* curves exhibited a clear two-step response corresponding to 2DEG at the AlGaN/GaN interface and electron accumulation at the upper AlON/AlGaN interface. Negligible *C*-*V* hysteresis and frequency dispersion clearly indicate excellent interface quality and sufficient immunity against charge injection into the gate dielectric. In addition, reduced interface state density (D_{it}) values as low as 1.2×10^{11} $cm^{-2}eV^{-1}$ and remarkably suppressed gate leakage current were successfully achieved with AlGaN/GaN MOS devices.

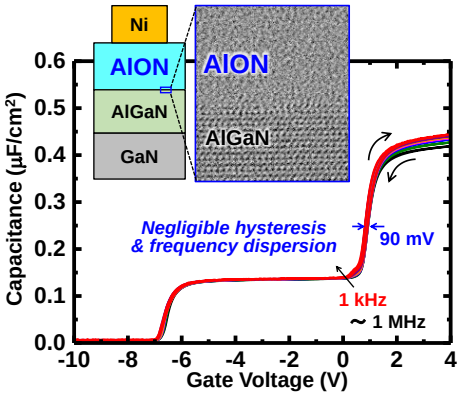

Fig. 2 Typical cross-sectional TEM image and bidirectional *C*-*V* curves obtained from AlGaN/GaN MOS capacitor with AlON gate dielectric. AlON film was directly deposited on AlGaN surface.

We also developed a novel method of producing high-quality CVD-AlON films by repeated ALD-based thin AlN deposition and subsequent *in situ* O_3 oxidation [6]. Moreover, by combining AlON gate dielectrics with advanced recessed-gate structures, high current and high voltage (20A/730V) normally-off AlGaN/GaN MOS-HFETs were successfully demonstrated [4].

3. Interface Engineering of GaN MOS Structures with GaO_x Interlayers

Oxidation of GaN surfaces forming GaO_x is a possible way of obtaining gate insulators for MOS devices. However, an insufficient conduction band offset at the interface and grain growth have been pointed out. Figure 3 shows typical surface morphology of GaN/Si and GaN/GaN substrates after thermal oxidation at 900°C in O_2 ambient [7]. The oxide grains were selectively formed at the threading dislocations on the epilayer, leading to rough surface morphology on the GaN/Si substrate (Fig. 3(a)). Contrary, when using GaN/GaN substrates, small oxide grains were densely distributed over the surface and morphology was significantly improved as shown in Fig. 3(b). A smaller RMS roughness value of 0.6 nm was observed even after thermal oxidation (3.7-nm-thick).

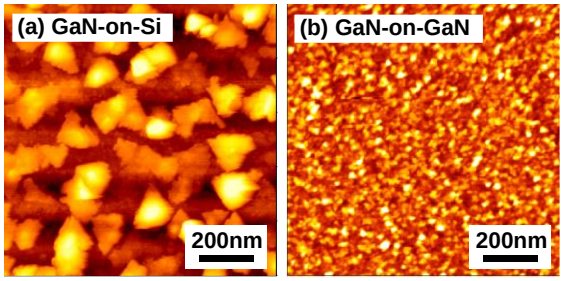

Fig. 3 AFM images of (a) GaN/Si and (b) GaN/GaN surfaces after thermal oxidation at 900°C for 30 min in dry O_2 ambient.

Based on this finding, we proposed GaN MOS devices with thin GaO_x interlayers, in which oxide interlayers were formed by oxidation of GaN surfaces or deposition prior to SiO_2 growth [8]. We also fabricated SiO_2/GaO_x/GaN stacked structures by optimizing conditions for plasma-enhanced CVD for SiO_2 [9]. Thin GaO_x layers were formed by radical oxidation of GaN at the initial stage of SiO_2 deposition, and subsequent annealing under appropriate conditions produced high-quality SiO_2/GaO_x/GaN stacked structures. Figure 4 shows *C-V* curves and oxide breakdown field of GaN MOS capacitors fabricated on the free-standing substrates. As shown in Fig. 4(a), well-behaved *C-V* curves with negligible hysteresis and frequency dispersion were obtained. Moreover, an extremely low D_{it} value (< 10^{10} $cm^{-2}eV^{-1}$) and improved reliability in terms of reproducibility and robustness against dielectric breakdown were demonstrated by the rapid thermal annealing at 800°C, as shown in Fig. 4(b).

Despite the excellent properties of n-type MOS capacitors, there remain major issues regarding reliability and process optimization, since thermal diffusion of Ga atoms from GaO_x interlayers significantly deteriorates reliability of gate stacks. Insertion of nitrogen-rich layers between the insulator/GaN interfaces, as well as rapid thermal process, is beneficial to suppress Ga diffusion [9,10]. The latest research also revealed that anomalous fixed charges due to oxygen vacancies in the GaO_x interlayers are generated by the reaction of GaO_x with hydrogen even at moderate temperatures [11]. Furthermore, there exist a significant amount of interface states near the valence band edge of GaN, which makes it difficult to realize hole accumulation of p-type MOS capacitors.

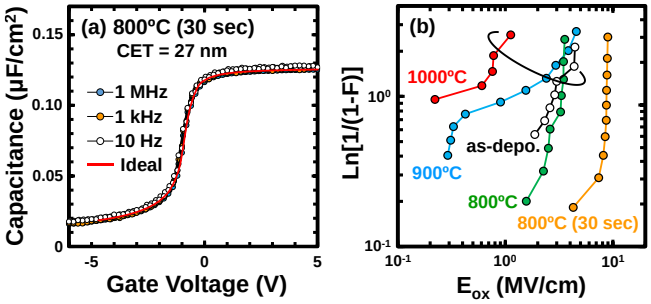

Fig. 4 Electrical properties of GaN MOS capacitors with SiO_2/GaO_x stacked gate dielectrics: (a) Multi-frequency *C-V* measurements, (b) Oxide breakdown field characteristics (Weibull plot) of GaN MOS devices depending on post annealing conditions.

4. Conclusions

In order to maximize performance of GaN-based power devices, advanced gate dielectrics are indispensable. For this purpose, the importance of suitable materials selection and interface engineering were discussed on the basis of recent findings. CVD-AlON films were found to be a well-balanced gate dielectric material in terms of interface and insulating properties. The ALD-based AlON deposition was proven to be beneficial for fabricating recessed-gate AlGaN/GaN MOS-HFETs. Regarding SiO_2/GaO_x/GaN gate stacks, thin GaO_x interlayers offered excellent electrical properties of n-type GaN MOS devices, but careful interface engineering is needed to ensure reliability of the MOS devices.

Acknowledgements

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