 Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp783-784

Mixed Signal Technology for 5G Era: History and Future

Akira Matsuzawa

Tech Idea Co., Ltd.
1-21-5-1, Shukugawara, Tamaku, Kawasaki, 214-0021, Japan
Phone: +81-44-385-2855 E-mail: matsu@techidea.co.jp

Abstract

The history of mixed signal technology for millimeter-wave adopted to 5G, centered on the development of the 60GH millimeter-wave CMOS transceiver is reviewed. The important technical points and future technology direction are also discussed.

1. Introduction

In 2007, we started the development of a millimeter-wave CMOS transceiver. At that time a simple transceiver using a GaAs MMIC was already prototyped. The simplest ASK modulation was used, and the data rate was about 1Gbps.

Wireless communication needs multi-level QAM modulation to increase the data rate, but wideband baseband circuit with high speed ADC is required. In addition, a stability of the oscillator was not sufficient.

As is often seen in technological development in Japan, device development preceded, and signal processing and system/circuit technology were not developed in parallel, to achieve the ultra-high data rate expected for millimeter waves. I decided the goal of this project was to develop not only a radio frequency circuit but also a baseband circuit to realize high data rate of over 10Gbps in millimeter waves.

2. Development scenario

The data rate in a communication is determined by the famous Shannon theorem, where M is the number of channels, BW is the signal bandwidth, P_s is the signal power, and P_n is the noise power.

$$D_{rate} = M \cdot BW \log_2\left(1+\frac{P_s}{P_n}\right) \qquad (1)$$

Therefore, to increase the data rate, it is necessary to increase the number of channels M, signal bandwidth BW, and P_s/P_n. When using N-bit QAM modulation, equation (1) is

$$D_{rate} \approx M \cdot BW \cdot N \qquad (2)$$

Therefore, it is necessary to increase the data rate so that modulation with a larger number of bits N can be used.

It is also very important to increase Equivalent Isotropic Radiated Power (EIRP) for sufficient P_s and to increase the number of channels, M by MIMO. Beamforming technology by multichip mounting on a planar antenna and phase shift was required. Development of this technology started late and was recently developed.

3. Transceiver chip

1) Low phase noise

In the development of the 60GHz CMOS transceiver, a large phase noise of the oscillator prevented the use of multilevel modulation. Phase noise of -90dBc/Hz@1MHz or less is necessary to realize 16QAM, but the phase noise of the quadrature 60GHz VCO at that time was as large as -76dBc/Hz@1MHz [1]. The reason for this is the low Q of LC tank of the 60GHz VCO. Therefore, as shown in Fig. 1, low phase noise of -95dBc/Hz@1MHz was realized by using injection lock technology that injects the output of 20GHz PLL with high Q into the 60GHz quadrature VCO [2]. As a result, we realized 64QAM and then realized 256QAM.

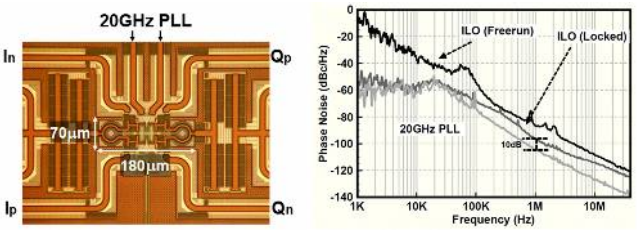

Fig. 1. Injection lock 60GHz QVCO and phase noise.

2) Broadband

We tried to widen the band by canceling the capacitance with a negative capacitance realized by a differential circuit, instead of conventional impedance matching using reactance elements that has a frequency characteristic essentially.

The first 60GHz CMOS transceiver was developed in 2011 [3]. Fig. 2 and Fig. 3 show the block diagram and chip layout of the 60GHz band CMOS transceiver announced in 2014 [4]. The direct conversion method achieved wide bandwidth and low power consumption.

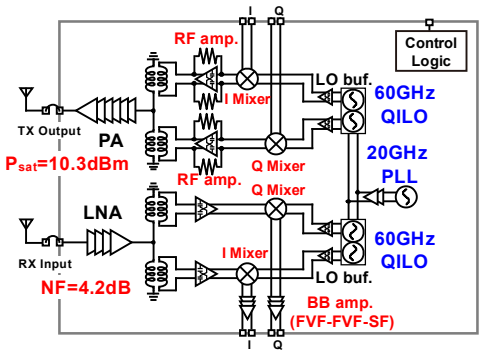

Fig. 2. 60GHz direct conversion CMOS transceiver.

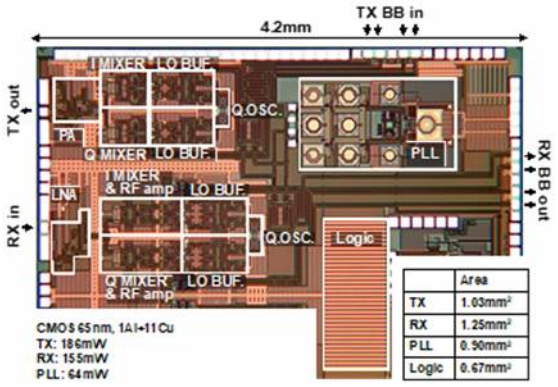

Fig. 3. 60GHz CMOS transceiver Chip.

3) Phase control

The millimeter wave needs phase sifting to realize beam forming to increase EIRP with multiple antennas. This technology is also indispensable for increasing data rate by increasing the number of channels, M by MIMO. Fig. 4 shows a block diagram of a multi-channel 28GHz bidirectional RX/TX circuit [5].

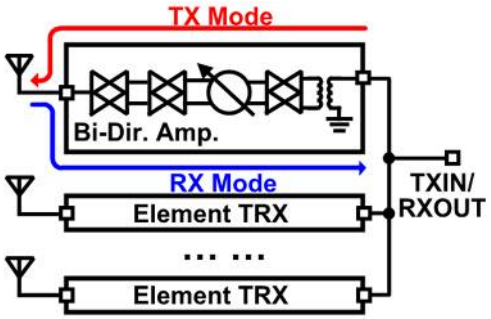

Fig. 4. Multi-channel 28GHz bidirectional RX/TX circuit.

4. Baseband circuit

Baseband circuits play an extremely important role in ultra-high-speed communication. ADC is especially important. Fig. 5 shows the effective resolution and error rate of the ADC in the 64QAM system. Only when the effective bits reached 7.15 bits, the error rate satisfy the specifications. Thus, the ADC performance has a great impact on the error rate. the ADC conversion method differs depending on the signal bandwidth and the required effective resolution.

If the bandwidth is about 1GHz and the resolution is 6 to 7 bits, the flash ADC is the easiest to realize. Flash ADC requires a large number of comparators, so power consumption has been a problem. Dynamic comparator that does not flow a steady current and digital error correction technology that suppresses the mismatch error are indispensable. in the case of 2.5GS/s, it came to operate with a power consumption of about 10mW [6]. An ADC with a resolution of 9 to 12 bits is required to handle 64QAM to 256QAM. The pipeline ADC is suitable for ADCs with a bandwidth of 200MHz to 400MHz. A 9bits, a 1.8GS/s 44mW ADC using an open-loop amplifier with linearity compensation has been developed [7].

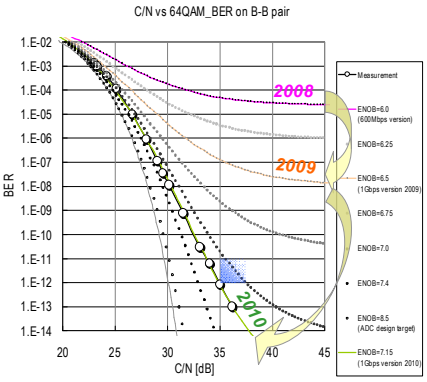

Fig. 5. ENOB of ADC and error rate in 64QAM.

5. Future technology direction

An over 100Gbps data rate will be required for 6G, and the carrier frequency will be increased to 300GHz. Since the f_{max} of CMOS is insufficient at such high frequencies, it is difficult to realize an amplifier, and an architecture using a frequency multiplier is being studied [8]. However, in some cases, a higher f_{max} compound device will be expected. Also, due to the need for beamforming and MIMO, a multiple antenna will be needed, but since the pitch is 0.5mm, which is 1/10 of the current one, fine integration technology for chips and antennas is required. The signal bandwidth will be several GHz, an ADC of over 10GS/s is required. SAR interleave ADC is a promising candidate, but improvement of the accuracy should be progressed. Furthermore, clock jitter of 100fs or less will be required, so low phase noise and low jitter oscillators and PLL technology are inevitable. In such a high-performance circuit, low power mixed signal technology should be continuously developed.

6. Conclusion

For ultra-high-speed wireless communication, increasing the bandwidth, SNR, the effective signal power, and the number of channels, M by MIMO are essential. To achieve this, a high frequency and low noise oscillator, high speed ADC, low power, and small area mixed signal technology should be developed continuously.

Acknowledgment

We would like to thank Professor Okada and Professor Miyahara.

References

[1] K. Scheir, et al., ISSCC, pp. 494-495, Feb. 2009.
[2] A. Musa, et al., A-SSCC, pp. 101–102, Nov. 2010.
[3] K. Okada, et al., ISSCC, pp.160-161, Feb. 2011.
[4] K. Okada, et al., ISSCC, pp. 346-347, Feb. 2014.
[5] J. Pang, et al., ISSCC, pp. 344-346, Feb. 2019,
[6] M. Miyahara, et al., RFIC, pp. 495-498, June 2012.
[7] L. Yu, et al., A-SSCC, 16-3, Nov. 2015.
[8] K. Takano, et al, ISSCC, pp.308-309, Feb. 2017.