D-3-03 Extended Abstracts of the 2021 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2021, pp217-218

High Breakdown Voltage (-580 V) in (001) Vertical-Type 2DHG Diamond MOSFET by p⁻-drift layer

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Abstract
We fabricated (001) vertical-type two-dimensional hole gas (2DHG) diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) with a p^--drift layer for the first time. Among the vertical diamond MOSFETs so far reported, we achieved the highest breakdown voltage (V_B: -580 V). The maximum drain current density of 210 mA/mm at L_{SD} of 17 μm was obtained. Compared to vertical diamond devices of the same L_{SD} without p^--drift layer, the drain current density was almost the same, but the breakdown voltage increased by more than 60 % (200 V). The implementation of the p^--drift layer was very effective for vertical diamond device.

1. Introduction
In power devices, vertical structure is suitable for both low on-resistance and integration, large current operation, and high breakdown voltage which are required for power MOSFETs. There is an urgent need to develop vertical p-channel power FETs compatible with n-type FETs for the realization of high-power and high-speed switching complementary inverters. We have reported vertical-type 2DHG diamond MOSFET using 2DHG which is induced independently of crystal orientation by C-H diamond surface and high temperature ALD-Al_2O_3[1][2][3]. However, the drift layer by p- layer has not been implemented because the controllability of lightly doping of boron into diamond is very difficult. In this work, we fabricated (001) vertical-type 2DHG diamond MOSFET with a p^--drift layer and achieved a breakdown voltage of V_B: -580 V, which is the highest among the vertical diamond MOSFETs currently reported.

2. General Instructions
The cross-sectional view of the vertical-type 2DHG diamond MOSFETs with p^--drift layer is shown in Fig.1. Fig.2 shows an optical micrograph of the vertical-type device and scanning electron microscope (SEM) image of the vertical-type device. A p^--drift layer was deposited on a p^+-type diamond substrate using the microwave plasma chemical vapor deposition (MPCVD) method. The thicknesses of the p^--drift layer ([N]: 1.0×10^{16} cm^{-3}, [B]: 8.0×10^{17} cm^{-3}) was 4.0 μm. A nominally undoped layer and a nitrogen-doped layer ([N]: 3.0×10^{18} cm^{-3}~8.0×10^{18} cm^{-3}) were deposited on a p^--drift layer by the MPCVD method. The thicknesses of the nominally undoped layer and the nitrogen-doped layer were 0.5 and 1.5 μm, respectively. The nitrogen-doped layer acts as a vertical current blocking layer. Then, 100 nm MgO is deposited as a trench etching mask, and trench with a depth (D_T) of 3 μm, a width (W_T) of 6 μm are formed by inductively coupled plasma reactive ion etching using O_2 plasma. After trench formation, a 300 nm regrown undoped layer was deposited by the MPCVD method to induce the 2DHG and secure the drift layer on the trench sidewall. Titanium, platinum, and gold (Ti/Pt/Au: 30/20/100 nm) were deposited as source electrodes and annealed in an H_2 atmosphere to form titanium carbide as source contacts. Then, the substrate surface was hydrogen-terminated by remote plasma treatment, and oxygen termination was then formed on the device, apart from the active area of the device, for electrical isolation. The 200-nm-thick Al_2O_3 was deposited as the gate insulator through the high-temperature atomic layer deposition (ALD) method and a drain electrode (Ti/Au: 10/250 nm) was deposited on the back surface of the substrate. Finally, aluminum (300 nm) was deposited as the gate electrode to complete the vertical-type device.

3. Results and Discussion
The source-gate length (L_{SG}), gate-trench (L_{GT}), gate-drain (L_{GD}), source-drain (L_{SD}) and gate length (L_G) for this device are 3 μm, 4 μm, 10 μm, 17 μm, 4 μm, respectively. As shown in Fig. 2, the area size of an active region for this device ($L_{SS} \times W_G = 7.5 \times 10^{-6}$ cm^2) is defined by multiplying the distance between the trench-side edges of two sources (L_{SS}: 30 μm) and the gate width (W_G: 25 μm). From the I_D-V_{DS} characteristics shown in Fig. 3, the maximum drain current density ($I_{D,max}$) normalized by the gate width is 210 mA/mm at V_{DS}: -50 V and V_{GS}: -20 V. In the active region, the $I_{D,max}$ is 1400 A/cm^2 and the on-resistance (R_{on}) is 23 mΩ· cm^2. The drain current density obtained in this study is comparable to that of a vertical device of the same device size without a p^--drift layer [1]. As shown in Fig. 4, no gate leakage current is observed at room temperature (300 K) and on/off ratio is about 6 orders of magnitude. As shown in Fig. 5, a high breakdown voltage (V_B): -580 V is achieved. This value is more than 60 % (200 V) higher than the breakdown voltage (V_B: -359 V) [1] of a device of the same size without a p^--drift layer, and is the highest value reported for vertical diamond FETs. From the above, it can be confirmed that the p-drift layer does not

significantly reduce the current value and increase the breakdown voltage. Further improvement of the breakdown characteristics can be achieved by increasing the p-drift layer thickness (4 µm at present) to about 10 µm in the near future. In addition, by introducing a trench gate structure [3] into this device structure, the device can be made smaller, and by implementing a high-density boron-doped layer under the source electrode [4], low on-resistance can be achieved, resulting in a p-type power trench diamond MOSFET with high breakdown voltage and low on-resistance.

4. Conclusions

We fabricated (001) vertical-type 2DHG diamond MOSFETs with a p^--drift layer and achieved a breakdown voltage of V_B: -580 V, which is the highest among the vertical diamond MOSFETs currently reported.

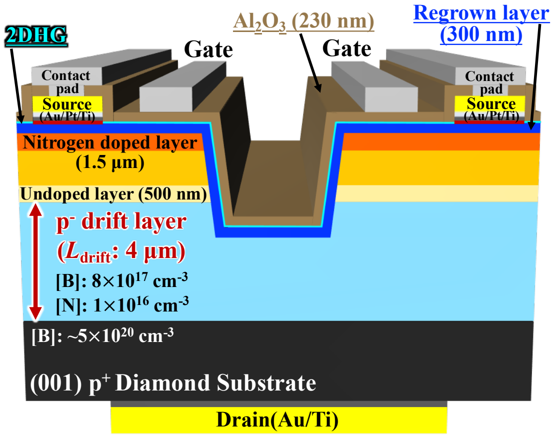

Fig.1 Cross-sectional view of the (001) vertical-type 2DHG diamond MOSFET with p^--drift layer (4 µm)

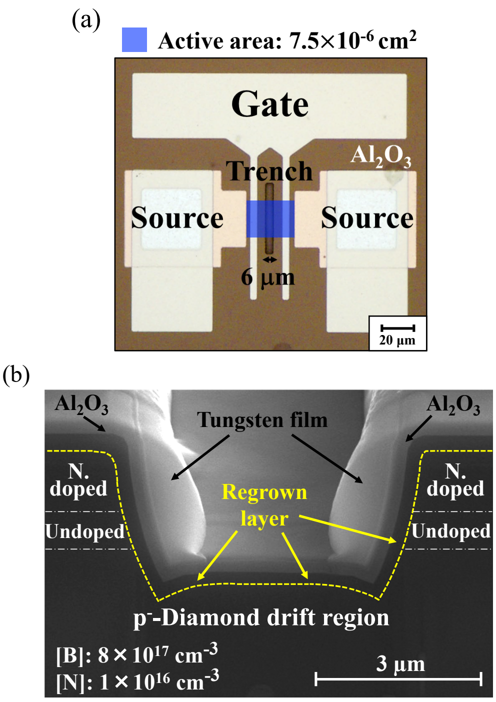

Fig.2 (a) An optical micrograph of the vertical-type device and (b) scanning electron microscope (SEM) image of the vertical-type device

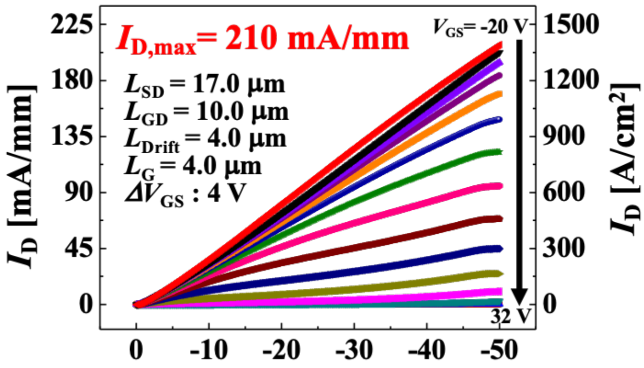

Fig.3 I_D-V_{DS} characteristics. The maximum drain current density was 210 mA/mm at V_{DS} and V_{GS} of –50 V and –20 V.

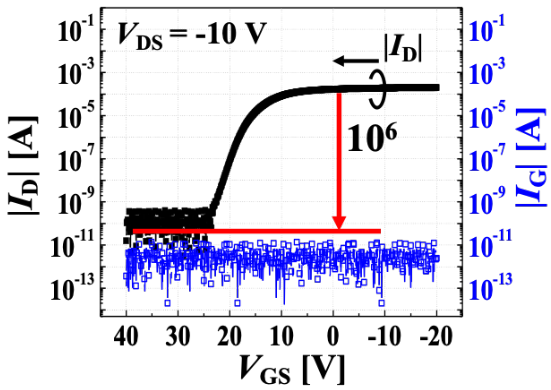

Fig.4 $|I_D|$-V_{GS} and $|I_G|$-V_{GS} characteristics for a V_{GS} of -20 to 40 V at a V_{DS} of -10 V (300 K). On/off ratio was 6 orders of magnitude.

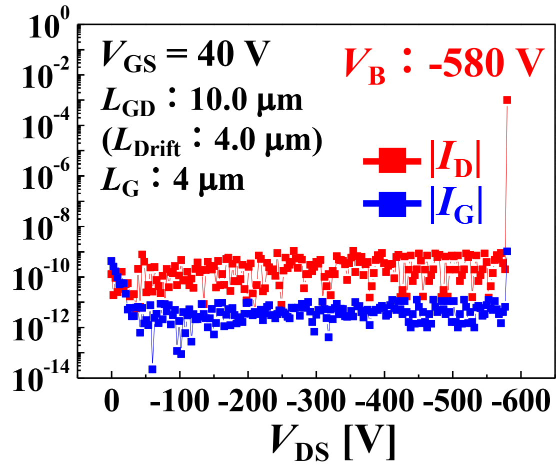

Fig.5 Breakdown characteristics of a device with L_{GD} = 10.0 µm at V_{GS} = 40 V. Breakdown voltage was -580 V

Acknowledgements

This study was partially supported by MEXT Project on Design & Engineering by Joint Inverse Innovation for Materials Architecture

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