Extended Abstracts of the 2021 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2021, pp221-222

Lowest contact resistance for high drain current density >1A/mm at Diamond MOSFETs with heavily boron-doped source and drain

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Abstract

We fabricated heavily boron-doped source and drain layers in MOSFETs to increase drain current density and reduce contact resistance between the source and two-dimensional hole gas (2DHG) layer. [1] ALD-Al_2O_3 diamond MOSFETs which have double-finger structures were investigated in DC and RF performances from the point of the contact resistance at the heavily boron-doped layer.

1. Introduction

Diamond has a wide band gap (5.5 eV), high thermal conductivity (22 W/cm・K), and high breakdown field. Therefore, Diamond is expected to apply RF amplifier. We fabricated high-voltage ALD-Al_2O_3 Diamond MOSFETs which accumulated Al_2O_3 (200 nm) as gate insulator by high temperature ALD process. Then we achieved the highest output power density P_{out} = 3.8 W/mm [2] in p-type FETs. High output power performance is critical for the radio frequency (RF) amplifier applications. It is valid for high output to reduce on-resistance, improve operating voltage $V_{DS,\,Q}$ and current density I_D, and increase actual current by extending the gate width. The device with extended W_G may deteriorate output current because of self-heating, and influence characteristics of devices caused by increase of gate resistance. In this work, we fabricated ALD-Al_2O_3 MOSFETs with a boron-doped layer on a pure (111) diamond and evaluated DC and RF performance as well as contact resistance in detail.

2. Device Information

Devices were fabricated on a pure (111) diamond. Fig.1 shows the sectional view of boron-doped diamond MOSFETs. We etched selectively by ICP-RIE through the evaporated metal mask to form space for heavily boron-doped epitaxial layer for source and drain. The thickness of the boron-doped layer was 150 nm. Source and Drain electrodes are deposited Ti/Pt/Au (20 nm/30 nm/90 nm). The thickness of Al_2O_3 gate insulator is 200 nm. And the gate length was fixed L_G = 1.0 µm and the source-drain length L_{SD} was fixed 3.0 µm. Fig.2 shows the model of top view of fabricated devices. We adopted double gate finger structure for the reduction of gate resistance. It can be implied from Fig.2.

3. Results and Discussion

Fig.3 shows the drain current-voltage characteristics of devices with W_G = 200 µm. At V_{GS} = -28 V and V_{DS} = -40 V, the maximum drain current density I_{Dmax} was 1.03 A/mm, R_{on} was 23 Ω mm. To obtain even higher current density, it is valid to shorten the distance between the source and drain, for example. It is expected that the drain currency density achieves 1.5 A/mm when L_{SD} is designated 0.5 µm. Such a minute device can be able to manufacture by using electron beam lithography when we coat resist of metal mask for boron-doped layer. Fig.4(a) and Fig.4(b) show TLM pattern on the substrate, (a) 2DHG and boron-doped layer and (b) only 2DHG without boron-doped layer. As for (a), contact resistance $R_{contact}$ was 1.77 Ω mm and sheet resistance R_{sheet} was 6.7 kΩ/sq. As for (b), $R_{contact}$ was 27.5 Ω mm and R_{sheet} was 16.8 kΩ/sq. These results suggest that boron-doped layer under the source and drain area reduce both contact resistance and sheet resistance. In addition to these patterns, in order to research contact resistance only between boron-doped layer and 2DHG, we designed a pattern like Fig.4(c) where only boron-doped layer is present. As for (c), $R_{contact}$ was 0.49 Ω mm and R_{sheet} was 64 Ω/sq. From these results, each element of resistance can be calculated. $R_{TiC\text{-}Boron}$ was 0.49 Ω mm, R_{Boron} was 0.32 Ω mm, $R_{Boron\text{-}2DHG}$ was 0.96 Ω mm. This result suggests that the obstruction between boron-doped layer and 2DHG is not a serious problem because the contact resistance (=0.96 Ω mm) is very small. Fig.5 shows the large signal performance of a device of W_G = 200 µm. It was evaluated by using a load pull system at 1 GHz. Power output density 3.6 W/mm was obtained on a device of W_G = 200 µm. This value is to be equal to the maximum value of Diamond MOSFETs (= 3.8 W/mm). Moreover, the maximum value was obtained in a device of W_G = 100 µm; that is, actual power in this experiment is twice than that of maximum value.

4. Conclusion

In this work, we fabricated boron-doped MOSFETs on a pure (111) diamond substrate and evaluated DC and RF performance as well as contact resistance between boron-doped layer and 2DHG. As a result, over 1 A/mm of drain current density was obtained. To obtain even higher current density, it is valid to shorten the distance between the source and drain. As for the TLM measurement, boron-doped layer reduced both contact resistance and sheet resistance. Then we found out that the obstruction between the boron-doped layer and 2DHG is not a serious problem because the contact resistance between them is as small as 0.96 Ω mm. As for the large signal performance, power output density 3.6 W/mm was obtained on a device of W_G = 200 μm. This is to be equal to the maximum value of Diamond MOSFETs, but actual output power is twice than that of maximum value.

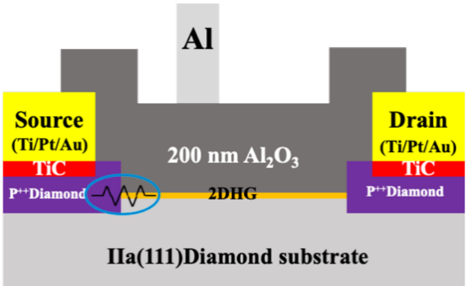

Fig.1 The sectional view of boron-doped diamond MOSFETs

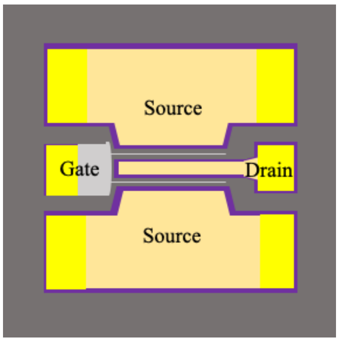

Fig.2 The model of top view of a device

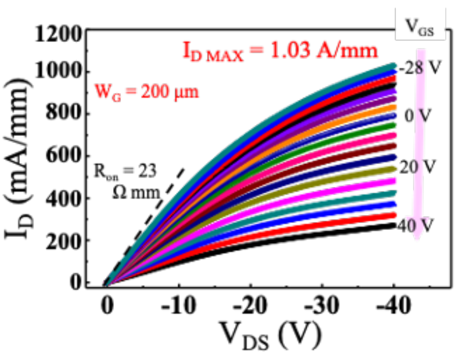

Fig.3 The drain current density
(W_G = 200 μm, V_{DS} = 0 to -40 V, V_{GS} = -28 to 40 V)

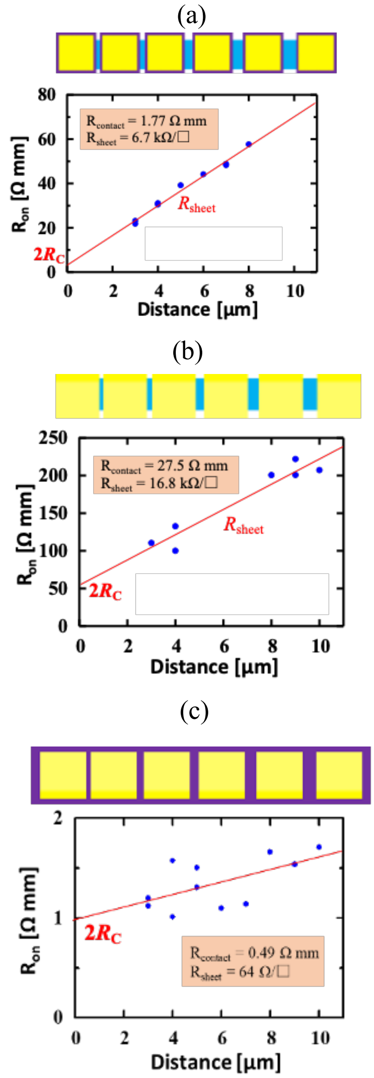

Fig.4 Results of TLM measurements
(a) with 2DHG and boron-doped layer (b) only 2DHG without boron-doped layer (c) with only boron-doped layer

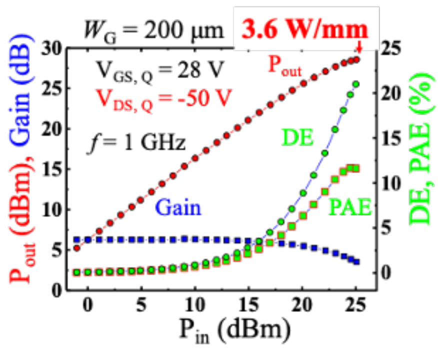

Fig.5 The large signal performance (W_G = 200 μm)

This work is supported in part by MEXT Project on Design & Engineering by Joint Inverse Innovation for Materials Architecture.

References

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