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Reduction of Interface State Density in the SiC MOS Structures by a Non-oxidation Process

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Abstract

A high density of interface states in SiC MOS structures has been a critical problem in the last several decades. We achieved substantial reduction of interface state density by adopting a "non-oxidation" process for gate-oxide formation. The concept and impacts of the proposed process are demonstrated.

1. Introduction

SiC has received increasing attention as a wide bandgap semiconductor suitable for high-voltage and low-loss power devices [1]. Through recent progress in SiC technology, 1–3 kV-class 4H-SiC power MOSFETs and Schottky barrier diodes have been commercialized, demonstrating remarkable reduction of power dissipation in various electric power systems. However, the on-resistance of 1 kV-class SiC power MOSFETs has been severely limited by the channel resistance due to the very poor channel mobility, as shown in Fig. 1 [2]. The keys for achieving the relatively low on-resistance in SiC power MOSFETs include reduction of the channel length, use of thinner gate oxides, and increase of the cell density by shrinking the cell pitch. However, these MOSFET designs cause the reliability concerns such as inferior short-circuit ruggedness and threshold voltage instability, due to the short-channel effects and higher oxide field, respectively. Thus, an innovative breakthrough in SiC MOS structures is strongly required.

In this paper, recent achievements in significant reduction of MOS interface state density (D_{it}) and enhancement of channel mobility are presented. One of the critical points is formation of SiO_2 by excluding thermal oxidation of SiC.

2. Oxide Formation without Thermal Oxidation of SiC

For a long time, thermal oxidation of SiC has been the standard method to form a gate oxide (SiO_2) for MOSFET fabrication. It has been believed that some carbon atoms must remain near the SiO_2/SiC interface and those carbon atoms may be the main origin of interface defects. In spite of extensive studies on physical and chemical analyses of the SiO_2/SiC structures, however, a consensus about the origin of interface defects has not been reached in the community.

In the meantime, several first-principles calculation studies on defects near the SiO_2/SiC interface [3,4] have revealed that a $(C\text{-}C)_C$ defect at the interface, a $(C\text{-}C)_{Si}$ defect inside SiC, and some other C-related defects have relatively low formation energy at a typical oxidation temperature (1200–1300°C) and these defects create electrically active levels in the bandgap near E_c. Based on this theoretical prediction and some other experimental facts [5], it is presumed that thermal oxidation of SiC inevitably induces generation of various C-related defects at and near the SiO_2/SiC interface.

Thus, we have exploited two different processes for gate-oxide formation while excluding thermal oxidation of SiC. Figure 2 shows the schematic process flows of gate oxide formation on SiC, where Fig. 2(a) is the conventional process and Figs. 2(b) and (c) illustrate the proposed processes to avoid thermal oxidation of SiC. In Fig. 2(b), a polycrystalline Si thin film is deposited on SiC and this Si film is converted to SiO_2 by thermal oxidation [6]. The temperature of Si oxidation for obtaining SiO_2 must be as low as possible (typically 750°C), so that SiC is never oxidized while Si is completely converted to SiO_2. In Fig. 2(c), a SiO_2 film is directly deposited on the SiC surface by chemical vapor deposition (CVD) [7]. In either case, H_2 etching of the SiC surface at about 1300°C prior to thin film deposition as well as interface nitridation after oxide formation are crucially important to fabricate a high-quality SiC MOS interface.

3. Defect Reduction in SiC MOS Structures

The energy distributions of interface state density obtained for several SiO_2/SiC(0001) MOS structures are plotted in Fig. 3 [8]. Here n-type MOS capacitors with an oxide thickness of about 30 nm were prepared, and the interface state density was extracted by a high(1 MHz)–low(quasi-static) method. "As-Ox" and "Ox-NO" denote the results for the conventional processes, namely oxide formation by thermal oxidation without and with post-oxidation annealing in NO, respectively. "H_2-CVD-N_2" and "H_2-CVD-NO" indicate those for the proposed processes shown in Fig. 2(c) with interface nitridation by N_2 and NO, respectively, where N_2 annealing was performed at 1450°C for 45 min and NO annealing at 1250°C for 70 min. By the proposed processes ("H_2-CVD-N_2" and "H_2-CVD-NO"), the interface state density can be reduced to a mid 10^{10} $cm^{-2}eV^{-1}$ near E_c. In the conventional processes ("As-Ox" and "Ox-NO"), the interface state density exhibits a rapid increase toward E_c, which is the main cause for the very low channel mobility in n-channel SiC(0001) MOSFETs. In contrast, such a sharp increase in the interface state density near E_c was not observed and the

distribution was rather flat in the measured energy range for the MOS structures formed by the proposed processes, implying that the defect nature may be different. At an energy level of E_c – 0.2 eV, the interface state density with the proposed processes is about four times lower than that for the conventional "Ox-NO". It is noted that an even lower interface state density of a low 10^{10} $cm^{-2}eV^{-1}$ can be achieved with the proposed process shown in Fig. 2(b) [6].

To investigate the impact of interface defect reduction on device characteristics, n-channel SiC(0001) MOSFETs were fabricated on p-type epitaxial layers with an acceptor density of 1-3×10^{15} cm^{-3}. Figure 4 demonstrates the channel mobility (field-effect mobility) versus the gate voltage for SiC MOSFETs with gate oxides formed with four different processes, the conventional ones ("As-Ox" and "Ox-NO") and the proposed ones ("H_2-CVD-N_2" and "H_2-CVD-NO") [8]. The peak mobility for the "Ox-NO" MOSFET is 41 cm^2/Vs, which is typical and has been unchanged in the last 20 years. Although the "H_2-CVD-N_2" MOSFET exhibited a high peak mobility of 85 cm^2/Vs, the threshold voltage was shifted to the negative direction, resulting in normally-on operation. On the other hand, a similar high peak mobility of 80 cm^2/Vs while keeping normally-off operation (threshold voltage: 0.92 V) was achieved with the "H_2-CVD-NO" MOSFET. The high mobility in n-channel MOSFETs reflects the low interface state density near the conduction band edge, which was attained by the proposed three-step process, (i) H_2 etching to remove a defective surface layer, (ii) oxide formation without oxidation of SiC, and (iii) interface nitridation.

In order to fabricate high-performance and high-reliability MOSFETs, high dielectric breakdown characteristics as well as the stability of threshold voltage against the high gate bias are required. The leakage current through the oxide formed by the proposed "H_2-CVD-NO" process was below the detection limit (10^{-9} A/cm^2) until 6 MV/cm and exhibited Fowler-Nordheim current with a barrier height of about 2.7 eV from 6 to 11 MV/cm. The breakdown electric field of the oxide was as high as 11.2 MV/cm.

4. Conclusions

The SiO_2 formation by excluding SiC oxidation could open a new platform for controlling high-quality SiC MOS interfaces and thereby enhance the performance of SiC power MOSFETs in the future.

Acknowledgements

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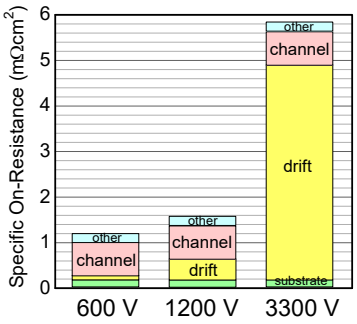

Fig. 1 Major components of specific on-resistance of 600, 1,200, and 3,300 V SiC power MOSFETs [2].

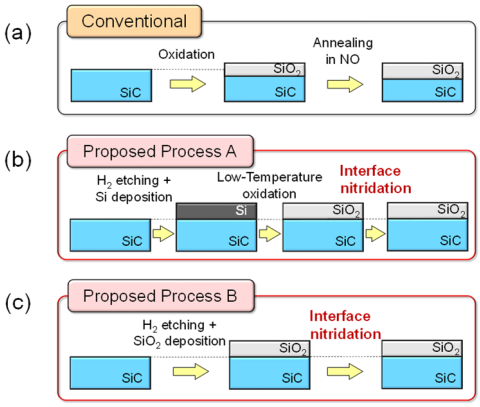

Fig. 2 Schematic process flows of gate oxide formation on SiC. (a) Conventional process. (b) and (c) illustrate the proposed processes to avoid thermal oxidation of SiC.

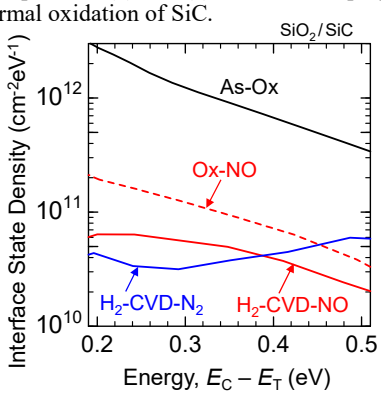

Fig. 3 Energy distributions of interface state density obtained for several SiO_2/SiC(0001) MOS structures, which were extracted by a high–low method on n-type MOS capacitors.

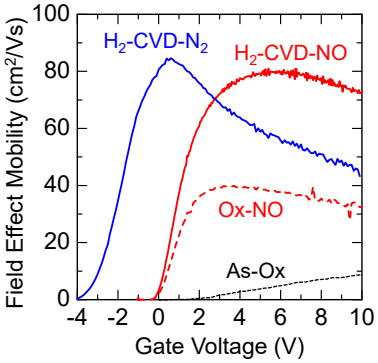

Fig. 4 Field-effect mobility versus the gate voltage for SiC MOSFETs with gate oxides formed with four different processes.