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Enhancement of Channel Mobility in 4H-SiC Trench MOSFET by Inducing Stress at SiO_2/SiC Gate Interface

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Abstract

To investigate the impact of stress in a SiO_2/SiC gate stack on the channel mobility of 4H-SiC trench MOSFETs, two variations of tensile-stress-induced SiC trench MOSFETs were fabricated by changing the deposition conditions of polycrystalline silicon for gate electrodes. The results found that μ_{eff} was enhanced by tensile stress. Based on the temperature dependence of mobility, all scattering mobilities were enhanced. It was supposed that the electron effective mass toward $[000\bar{1}]$ decreased because of the tensile stress toward $[1\bar{1}00]$.

1. Introduction

4H-SiC is regarded as an attractive new material for power MOSFETs because of its high breakdown voltage. However, when this material is used for MOSFETs, it results in insufficient channel mobility that must be enhanced. The effects of stress induced at the interface on effective channel mobility (μ_{eff}) are being investigated. It was recently reported that the μ_{eff} of a 4H-SiC (0001) lateral MOSFET could be enhanced by external compressive stress [1]. Consequently, this study fabricated two variations of tensile-stress-induced SiC trench MOSFETs by changing the deposition conditions of the polycrystalline silicon that is fabricated as a gate electrode. The stress around the gate stack and μ_{eff} were then evaluated.

2. Experimental methods

A n-type drift layer was formed on an n^+-type 4H-SiC (0001) substrate. Its donor concentration was about 1×10^{16} cm^{-3}. p-type and n^+-type layers were fabricated as body and source layers by ion implantation. The acceptor concentration of the body layer was about 1×10^{17} cm^{-3}. The trench gate was fabricated by dry etching so that the n-channel was located on the $(1\bar{1}00)$ face. A 75 nm-thick-SiO_2 was deposited followed by nitridation in a NO atmosphere. After that, phosphorus-doped polycrystalline silicon was deposited under two conditions (A and B) as the gate electrode, respectively.

The stress around the gate stacks was evaluated by cross-sectional Raman measurement with a 457.9 nm laser. The stress toward $[000\bar{1}]$ and $[1\bar{1}00]$ was calculated separately from the FTO(2/4)E2 and FTO(0)A1 Raman shift.[2]

The I_D-V_G characteristics were measured at a drain voltage of 0.1 V and a temperature between 233 and 573 K. The threshold voltage (V_{th}), interface state density (D_{it}) and μ_{eff} were then calculated from the I_D-V_G characteristics. V_{th} was determined from the ideal I_D-V_G curve [3]. Then, D_{it} was calculated from the subthreshold swing [4]. In the calculation of μ_{eff}, the parasitic series resistance was removed [5]. In SiC-MOSFETs, μ_{eff} can be divided into three components based on the scattering factors, namely the Coulomb scattering mobility (μ_C), optical phonon scattering mobility (μ_{opt}), and surface roughness scattering mobility (μ_{SR}) [6]. These scattering mobility values were calculated from the temperature dependence of μ_{eff} versus the effective field (E_{eff}).

3. Results and discussion

3.1 Evaluation of stress around the gate stack

Fig. 1 shows the stress toward $[1\bar{1}00]$ mapping images of cross-sectional trench MOSFETs in which polycrystalline silicon was fabricated under conditions A and B.

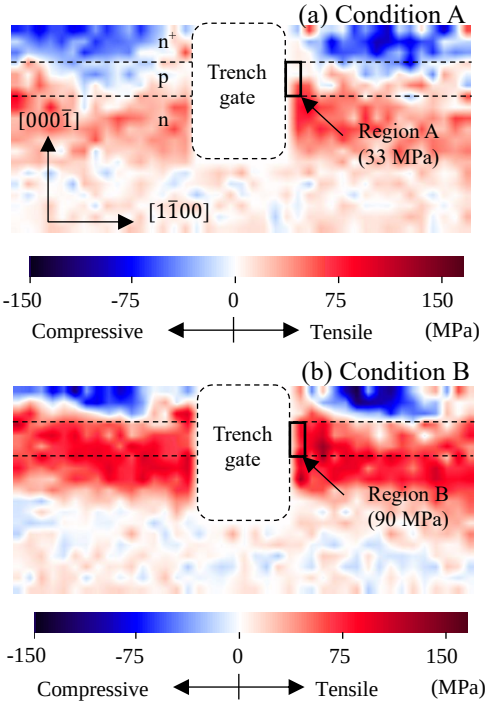

Fig. 1. The stress toward $[1\bar{1}00]$ mapping images of cross-sectional trench MOSFETs in which polycrystalline silicon was fabricated under condition A (a) and B (b). The average of the stress in regions A and B is shown.

The tensile stress of region B is 57 MPa higher than that of region A. In contrast, the stress toward the $[000\bar{1}]$ of region B is equivalent to that under condition A.

3.2 Electrical characteristics

Fig. 2 shows μ_{eff} at a temperature of 298 K as a typical result. The results of 9 chips picked from each wafers are shown. From the I_D-V_G measurements, it was found that the μ_{eff} at E_{eff} = 1 MV/cm under condition B (high stress) was 1.2 to 4.8% higher than under condition A (low stress). There are three possible reasons for this enhancement in μ_{eff}. The first is an increase in free electron density, the second is an enhancement in specific scattering mobility, and the third is an improvement in free electron mobility. From Fig. 3, the V_{th} and D_{it} under condition B are approximately equal to those under condition A. This means that there are no significant differences in the free electron density between conditions A and B. Fig. 4 shows the three scattering mobilities. Both μ_{opt} under condition B, which was the dominant factor of μ_{eff} at high temperature, and μ_C, which was the dominant factor at low temperature, increased by 0.9 to 5.1% compared to under condition A. Based on first principal calculation, F.M. Steel et al. reported that the electron effective mass is affected by strain [7]. Therefore, rather than an increase in the specific scattering mobility, it is supposed that the enhancement in μ_{eff} results from an improvement in the common terms of the scattering mobilities, and that the decrease in the electron effective mass toward $[000\bar{1}]$ is caused by the tensile stress toward $[1\bar{1}00]$.

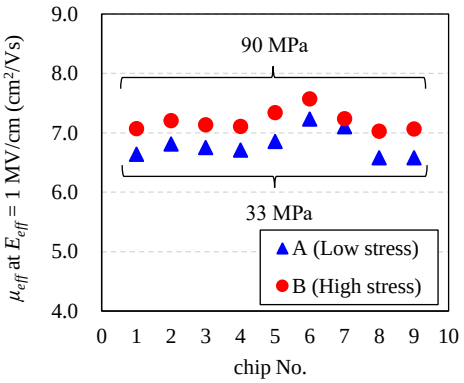

Fig. 2. μ_{eff} at E_{eff}=1 MV/cm at 298K was plotted. Chip No. corresponds to the position on the wafer.

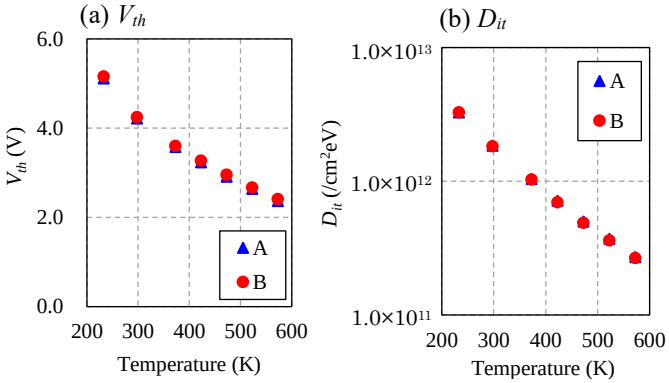

Fig. 3. The temperature dependence of (a) V_{th} and (b) D_{it}.

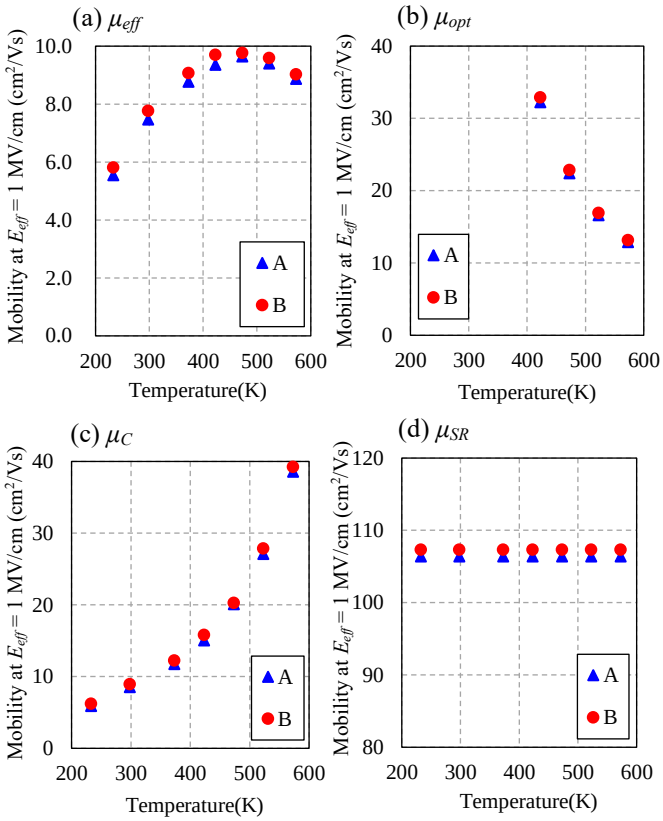

Fig. 4. The scattering mobility values were calculated from the temperature dependence of μ_{eff}. Each mobility at E_{eff}=1 MV/cm was plotted. (a) μ_{eff}, (b) μ_{opt}, (c) μ_C and (d) μ_{SR}.

4. Conclusions

It was found that the channel mobility changed due to stress in a 4H-SiC trench MOSFET. Mobility was particularly enhanced by the tensile stress toward $[1\bar{1}00]$. It was supposed that the enhancement effect was caused by a decrease in the effective electron mass toward $[000\bar{1}]$.

References

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